12/04/2002

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  File  94:JICST-EPlus  1985-2002/Sep W5
         (c)2002 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Oct
         (c) 2002 The HW Wilson Co.
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  File 103:Energy SciTec  1974-2002/Nov B2
         (c) 2002 Contains copyrighted material
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Set     Items   Description
S1     489594   (SILICON OR SI)(W)(DIOXIDE OR O2) OR SILICA OR MYRICKITE OR
                 TRIDYMITE OR BOBKOVITE OR MOGANITE OR QUARTZ OR CRISTOBALITE
                OR ADELITE OR ACTICEL
S2      79885   ACEMATT OR STISHOVITE OR COESITE OR SIBELITE OR CRYSVARL OR
                 CRYSTOBALITE OR SARDONYX OR QUARTZINE OR SIKRON OR MILLISIL -
                OR ROCK(W)CRYSTAL OR SIO2
S3       7228   CI=(SI SS(S) O SS)(S)NE=2
S4     123091   (SILICON OR SI)(W)(NITRIDE OR N OR MONONITRIDE) OR SIN OR -
                SILYLIUM
S5       2936   CI=(SI SS(S) N SS)(S)NE=2
S6    1756512   IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT? ?)) OR (MI-
                CRO)(W)(CIRCUIT? ? OR CHIP? ? OR ELECTRONIC?) OR CHIP? ? OR M-
                ICROCIRCUIT? ? OR DIE? ? OR LOGIC(W) CIRCUIT? ? OR WAFER? ? OR
                 MICROELECTRONIC? OR DICE
S7      72622   CC=B2570   Semiconductor integrated circuits
S8     171802   TRANSISTOR
S9     287822   BURY??? OR BURIED OR ENCAPSUL? OR CAPSUL? OR ENCAS?????
S10    203899   (HEXSIL OR METASILICON OR POLYSILICONCN OR SICOMILL OR SIL-
                GRAIN OR SILICON OR SILSO OR SI OR L44)(2N)(LAYER? OR FILM? OR
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S11       124   AU=(BRYANT, ANDRES OR BRYANT ANDRES OR BRYANT, A OR BRYANT
               A)
S12         7   AU=(JAFFE, M D OR JAFFE M D OR JAFFE, MARK D OR JAFFE MARK
               D)
S13       131   S11 OR S12
S14         0   S13 AND (S1:S3) AND (S4:S5)
S15      8304   (S1:S3) AND (S4:S5)
S16       310   S15 AND S8
S17        90   S16 AND (S6:S7)
S18        13   S17 AND DRAIN
S19         1   S17 AND DRAINS
S20        19   S17 AND SOURCE
S21         6   S17 AND S9
S22        27   S17 AND S10
S23        43   S18:S22
S24        36   RD (unique items)
S25        47   S17 NOT S23
S26        42   RD (unique items)
S27    203228   TRANSISTORS  (January 1969)
S28       421   S15 AND S27
S29        89   S28 AND (S6 OR S7)
S30        10   S29 AND DRAIN? ?
S31        15   S29 AND SOURCE
S32         3   (S30 OR S31) NOT S23
S33     89522   (S8 OR S27) AND (S6 OR S7)
S34       133   S33 AND S15
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               3N)(OXIDE OR INSULAT? OR DIELECTRIC)
S36         1   S34 AND S35
S37       562   S33 AND S35
S38         1   S37 AND S15
S39       221   S37 AND S10
S40         2   S16 AND S35
S41        37   S15 AND S35
S42         8   S41 AND (S6 OR S7)
S43         2   S41 AND S8
S44        13   (S43 OR S42 OR S40 OR S38 OR S36 OR S32) NOT S23
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24/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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6534187 INSPEC Abstract Number: A2000-08-8780B-009, B2000-04-7230J-012
Title: Development of sensors for direct detection of organophosphates. II. Sol-gel modified field effect **transistor** with immobilized organophosphate hydrolase
Author(s): Flounders, A.W.; Singh, A.K.; Volponi, J.V.; Carichner, S.C.; Wally, K.; Simonian, A.S.; Wild, J.R.; Schoeniger, J.S.
Author Affiliation: Chem. & Radiat. Detection Lab., Sandia Nat. Labs., Livermore, CA, USA
Journal: Biosensors & Bioelectronics vol.14, no.8-9 p.715-22
Publisher: Elsevier,
Publication Date: Dec. 1999 Country of Publication: UK
CODEN: BBIOE4 ISSN: 0956-5663
SICI: 0956-5663(199912)14:8/9L.715:DSDD;1-J
Material Identity Number: N695-1999-008
U.S. Copyright Clearance Center Code: 0956-5663/99/$20.00
Language: English
Abstract: For pt. I see ibid., vol. 14, no. 8-9, p. 703-13 (1999). pH-sensitive field effect transistors (FET) were modified with organophosphate hydrolase (OPH) and used for direct detection of organophosphate compounds. OPH is the organophosphate degrading gene product isolated from Pseudomonas diminuta. OPH was selected as an alternative to acetylcholinesterase, which requires inhibition mode sensor operation, enzyme regeneration before reuse, long sample incubation times, and a constant **source** of acetylcholine substrate. OPH was covalently immobilized directly to the exposed **silicon nitride** gate insulator of the FET. Alternatively, **silica** microspheres of 20 or 200 nm were formed via a base catalyzed sol-gel process and were dip-coated onto the gate surface; enzyme was then covalently immobilized to this modified surface. All sensors were tested with paraoxon and displayed rapid response (<10 s), with a detection limit of approximately 1*10/sup -6/ molar. The 200 nm sol-gel gate modification enhanced the signal of enzyme-modified devices without effecting device pH sensitivity. Sensors were stored at 4 degrees C in buffer and tested multiple times. Devices coaled with 200 nm **silica** microspheres maintained significant enzymatic activity over a period of 10 weeks while uncoated devices lost all enzyme activity during the same period. The 20 nm sol-gel modification did not enhance device response or enzyme stability. Successful reuse of sensor **chips** was demonstrated after stripping inactive enzyme with an RF oxygen plasma system and reimmobilizing active enzyme.
Subfile: A B
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24/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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4578234 INSPEC Abstract Number: B9402-2560R-033
Title: High-current and low acceleration voltage arsenic ion implanted polysilicon-gate and **source-drain** electrode Si MOS **transistor**
Author(s): Saito, Y.; Sugimura, Y.; Sugihara, M.
Author Affiliation: Nichiden-Toshiba Info. Syst. Inc., Kawasaki, Japan
Conference Title: Beam Solid Interactions: Fundamentals and Applications Symposium p.313-18
Editor(s): Nastasi, M.; Harriott, L.R.; Herbots, N.; Averback, R.S.

Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1993 Country of Publication: USA xvii+913 pp.
Conference Date: 30 Nov.-4 Dec. 1992 Conference Location: Boston, MA, USA
Language: English

Abstract: The fabrication process of high current arsenic (As) ion implanted poly-silicon (Si) gate and **source-drain** (SD) electrode **Si n**-channel metal-oxide-semiconductor field-effect-**transistor** (MOSFET) was examined. Poly-**Si film** n-type doping was performed by using high current (typical current: 2 mA) and relatively low acceleration voltage (40 keV) As ion implantation technique (Lintott series 3). It was observed that high dose-As implanted poly-**Si films** as is show refractoriness against radical fluorine excited by microwave. Using GCA MANN4800 (m/c ID No.2, resist: OFPR) mask pattern printing technique, the high current As ion implantation technique and radical fluorine gas phase etching (Chemical dry etching: CDE) technique, the n-channel poly-Si gate (rho s= approximately=100 Omega / Square Operator) enhancement MOSFETs (rho s-**source-drain**= approximately=50 Omega / Square Operator , **SiO2** gate=380 AA) with off-leak-less were obtained on 3" Czochralski-grown 2 Omega cm boron-doped p-type **wafers** (Osaka titanium). By the same process, a 8-bit single **chip** mu -processor with 26 MHz full operation was performed.
Subfile: B

24/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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02481609 INSPEC Abstract Number: A85077691, B85043335
Title: Implantable ion-sensitive transistors
Author(s): Harame, D.L.; Shott, J.D.; Bousse, L.; Meindl, J.D.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: Frontiers of Engineering and Computing in Health Care - 1984. Proceedings - Sixth Annual Conference of the IEEE Engineering in Medicine and Biology Society (Cat. No. 84CH2058-6) p.444-9
Editor(s): Semmlow, J.L.; Welkowitz, W.
Publisher: IEEE, New York, NY, USA
Publication Date: 1984 Country of Publication: USA viii+857 pp.
U.S. Copyright Clearance Center Code: CH2058-6/84/0000-0444$01.00
Conference Sponsor: IEEE
Conference Date: 15-17 Sept. 1984 Conference Location: Los Angeles, CA, USA
Language: English
Abstract: The optimization of ion-sensor transducers for long-term implantable pH sensing applications has been achieved by increasing the stability and linearity of the ion-sensitive field effect **transistor** (ISFET) through the use of multiple site materials, providing an on-**chip** Ag/AgCl reference electrode, and improving **encapsulation** reliability by junction-isolating the ISFET device. The device also features polysilicon interconnects to the **source** and **drain** and borosilicate glass as the pH sensitive gate dielectric material. Borosilicate glass has several advantages over **silicon nitride** and **silicon dioxide** ISFETs. It is a stable dielectric in the presence of aqueous solutions, the response does not degrade with time, and it can be easily made from materials common to **IC** fabrication technology. Two site models are developed to model the borosilicate glass and **silicon nitride** devices. Using materials with more than one type of site is shown to be a reliable method for achieving a linear nernstian response.

12/04/2002

Subfile: A B

24/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
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02290121 INSPEC Abstract Number: B84042160
Title: Silicide stiffened SFET **source/drains**
Author(s): Roberts, S.; White, F.R.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.26, no.10A p.5234-5
Publication Date: March 1984 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: This article describes a process for forming self-aligned silicide field-effect **transistor** (SFET) structures which are compatible with the use of gate structures including a **silicon dioxide-silicon nitride** combination.
Subfile: B

24/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC
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02256324 INSPEC Abstract Number: B84030756
Title: CMOS to reduce **chip** size by a third
Journal: Integrated Circuits International vol.7, no.12 p.11-13
Publication Date: Feb. 1984 Country of Publication: UK
CODEN: ICIIDZ ISSN: 0263-6522
Language: English
Abstract: The Swiss company Faselec have developed a new CMOS process called SACMOS (self-aligned contact CMOS) which achieves the same density with 4-micron minimum design rules as can be had with conventional CMOS designs using 2.5 mu m rules. Besides providing the higher density, Faselec's new technology simplifies layout considerably. SACMOS is based on the LOCOS (local oxidation on Si) CMOS technology that Faselec's parent company, Philips, pioneered in the 1960s. It begins with all the steps involved in the conventional CMOS process, after which nitrogen implantation is employed, followed by a thermal treatment to produce a **silicon nitride layer**. This layer serves as an oxidation barrier in the subsequent thermal oxidation steps. A **silicon dioxide layer** about 3000 angstroms thick is formed at the sides of the polysilicon gate electrode. At this point, the electrode is fully isolated-on top by the **silicon nitride** and on the sides by the 3000 angstrom Si/sub 2/O layer, thereby preventing shorts. It is with this isolating layer that the **drain** and **source** contacts align themselves, resulting in a no-clearance, space-saving MOS **transistor** configuration.
Subfile: B

24/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC
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00843735 INSPEC Abstract Number: B76001062, C75028710
Title: Making a one-device memory cell
Author(s): Kalter, H.L.; Vanderslice, W.B., Jr.
Author Affiliation: IBM, Armonk, NY, USA

12/04/2002

Journal: IBM Technical Disclosure Bulletin vol.18, no.4 p.1019-20
Publication Date: Sept. 1975 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: Leakage control in a memory cell is provided by placing a field shield over recessed oxide. The method also lends itself to reduced bit line capacitance. An array of these memory cells, each of which includes f.e.t. and a storage capacitor, is made by first forming a 50 AA **layer** of **silicon dioxide** over a silicon surface followed by a first 250 AA **layer** of **silicon nitride**. A recessed oxide pattern is formed in the silicon surrounding the **drain**, gate and **source** regions of the **transistor**, by etching through the **silicon nitride** and **silicon dioxide** into the surface of the silicon. **Silicon dioxide** is then thermally grown in the etched region of the silicon, up to the original surface of the silicon to produce the recessed oxide.
Subfile: B C

24/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

00486508 INSPEC Abstract Number: B73008691, C73005274
Title: Field-effect **transistor** memory circuit
Author(s): LeBlanc, A.R.
Journal: IBM Technical Disclosure Bulletin vol.15, no.4 p.1292-3
Publication Date: Sept. 1972 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: This random-access memory circuit uses a layer of high-dielectric material, such as **silicon nitride** , in the storage capacitor to reduce the size of each memory cell area. The circuit includes a field-effect **transistor** formed in, for example, a P-type silicon **wafer** with suitable spaced apart N-type regions and a gate electrode disposed between regions on a **layer** of **silicon dioxide** . A metallic electrode contacts one surface of the Si/sub 3/N/sub 4/ layer, while the other surface of this layer is in contact with an N-type region. A word line driver, connected to a gated electrode applies control pulses to the field-effect **transistor**, and a bit line driver and sense amplifier is used to write binary information into and read information out of the storage capacitor.
Subfile: B C

24/3,AB/8 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
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0730853 NTIS Accession Number: AD-D005 272/0/XAB
MNOS Memory **Transistor** having a Redeposited **Silicon Nitride** Gate Dielectric
(Patent)
Blaha, F. C. ; Cricchi, J. R.
Department of the Air Force Washington DC
Corp. Source Codes: 109850
Report No.: PAT-APPL-707 574; PATENT-4 096 509
Filed 22 Jul 76 patented 20 Jun 78 8p
Languages: English Document Type: Patent
Journal Announcement: GRAI7902
Supersedes PAT-APPL-707 574-76, AD-D003 057.

This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of patent available Commissioner of Patents, Washington, DC 20231 $0.50.

NTIS Prices: Not available NTIS

A processing technique, using two separate **silicon nitride** depositions (one to form the memory regions and the second to form the nonmemory regions), is used to provide a radiation hard **drain source** protected memory **transistor**. The amount of **silicon dioxide** used in the nonmemory regions is also minimized. A typical device comprises a mesa etched from a silicon-on-sapphire (SOS) **wafer** into which P+ **source** and **drain** regions are implanted. A 100 A **layer** of **silicon dioxide** and a second 1000 A **layer** of nonmemory **silicon nitride** covers the mesa. The two layers are etched to define a substrate gate window. The gate window is covered by a 25 A layer of tunneling oxide. A final 500 A **layer** of memory **silicon nitride** covers the mesa structure. Contact windows are etched to accommodate **source, drain** and gate interconnect electrodes. (Author)

24/3,AB/9 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS
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0613266 NTIS Accession Number: AD-815 152/4/XAB

Single Crystal **Silicon Films** on Insulating Substrates (Follow on Program)

(Rept. for 1 Feb-30 Apr 67)

Autonetics Anaheim Calif

Corp. Source Codes: 048100

Report No.: C7-526.1/501

31 May 67 51p

Journal Announcement: GRAI7710

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NTIS Prices: PC A04/MF A01

Application of the techniques of ion injection doping to the fabrication of junction structures in silicon-on-sapphire has continued, employing both boron and sodium ion beams for acceptor and donor impurity doping, respectively. Some additional details of the injected impurity profile in silicon-on-sapphire relative to that in bulk single-crystal silicon have been acquired. A measure of the rate of diffusion of injected interstitial sodium ions in the silicon-on-sapphire crystal lattice has been obtained; the diffusion appears to be more rapid than in the bulk material. Further experiments with various combinations of masking materials for device fabrication have clearly demonstrated the value of the multilayer mask, especially that with molybdenum over **silicon dioxide** or over **silicon nitride** . Corollary efforts on development of improved ion sources for use on this program have produced encouraging results. Additional process development has been performed on a complementary MOS flip-flop memory cell. Power measurements on these cells have shown an average standby dissipation of 0.5 microwatt. Experiments were performed demonstrating a technique for controlling the threshold voltage of a MOS **transistor** . This technique should be useful where complementary devices are required.

24/3,AB/10 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

12/04/2002

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0585865 NTIS Accession Number: AD-D003 057/7/XAB
Radiation Hardened MNOS Memory **Transistor** and Method of Manufacture (Patent Application)
Blaha, F. C.
Department of the Air Force Washington D C
Corp. Source Codes: 109850
Report No.: PAT-APPL-707 574
Filed 22 Jul 76 14p
Document Type: Patent
Journal Announcement: GRAI7701
This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of application available NTIS. Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
The patent application relates to a processing technique using two separate **silicon nitride** depositions (one to form the memory regions and the second to form the nonmemory regions), employed to provide a radiation hard **drain source** protected memory **transistor**
. The amount of **silicon dioxide** used in the nonmemory regions is also minimized. A typical device comprises a mesa etched from a silicon-on-sapphire (SOS) **wafer** into which P+ **source** and **drain** regions are implanted. A 100 A **layer** of **silicon dioxide** and a second 1000 A **layer** of nonmemory **silicon nitride** covers the mesa and the two layers are etched to define a substrate gate window. The gate window is covered by a 25 A layer of tunneling oxide. A final 500 A **layer** of memory **silicon nitride** covers the mesa structure. Contact windows are etched to accommodate **source**, **drain** and gate interconnect electrodes.

24/3,AB/11 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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05850786
E.I. No: EIP01276572464
Title: Dual-metal gate CMOS technology with ultrathin **silicon nitride** gate dielectric
Author: Yeo, Y.-C.; Lu, Q.; Ranade, P.; Takeuchi, H.; Yang, K.J.; Polishchuk, I.; King, T.-J.; Hu, C.; Song, S.C.; Luan, H.F.; Kwong, D.-L.
Corporate Source: Dept. of Elec. Eng./Computer Sci. University of California, Berkeley, CA 94720, United States
Source: IEEE Electron Device Letters v 22 n 5 May 2001 2001. p 227-229
Publication Year: 2001
CODEN: EDLEDZ ISSN: 0741-3106
Language: English
Abstract: We report the first demonstration of a dual-metal gate complementary metal oxide semiconductor (CMOS) technology using titanium (Ti) and molybdenum (Mo) as the gate electrodes for the N-metal oxide semiconductor field effect transistors (N-MOSFETs) and P-metal oxide semiconductor field effect transistors (P-MOSFETs), respectively. The gate dielectric stack consists of a silicon oxy-nitride interracial **layer** and a **silicon nitride** (Si//3N//4) dielectric layer formed by a rapid-thermal chemical vapor deposition (RTCVD) process. C-V characteristics show negligible gate depletion. Carrier mobilities comparable to that predicted by the, universal mobility model for

silicon dioxide (SiO//2) are observed. 11 Refs.

24/3,AB/12 (Item 2 from file: 8)
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05837827
E.I. No: EIP01236529368
Title: Highly reliable poly-SiGe/amorphous-Si gate CMOS
Author: Uejima, K.; Yamamoto, T.; Mogami, T.
Corporate Source: Silicon Systems Research Labs. System Device and Fundamental Res. NEC Corporation, Sagamihara, Kanagawa 229-1198, Japan
Conference Title: 2000 IEEE International Electron Devices Meeting
Conference Location: San Francisco, CA, United States Conference Date: 20001210-20001213
E.I. Conference No.: 58091
Source: Technical Digest - International Electron Devices Meeting 2000. p 445-448 (IEEE cat n 00CB37138)
Publication Year: 2000
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: We have developed highly reliable poly-SiGe-gated CMOS devices using a poly-SiGe/a-Si (3 nm) gate structure for sub-0.1mum CMOS devices. It was found that by adding a thin amorphous-**Si** (a-**Si**) **layer**, Q//B//D(50%) is improved compared with the conventional poly-SiGe and even with pure poly-**Si** **N**/PMOS devices. Furthermore, low gate depletion was obtained for the poly-SiGe/a-Si gate. The polarity dependence of the Q//B//D improvement suggests that the a-**Si layer** reduces a "weak reliability layer" of SiO//2 near the SiGe/SiO//2 interface. Appreciably higher performance of poly-SiGe/a-Si gate N/PMOSFETs was demonstrated compared with conventional poly-Si gate N/PMOSFETs. 7 Refs.

24/3,AB/13 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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05476528
E.I. No: EIP00025024283
Title: Single **wafer** CVD of **silicon nitride** for CMOS gate applications
Author: Pomarede, C.; Werkhoven, C.; Weidmann, J.; Bergman, T.; Gschwandtner, A.; Houssa, M.
Corporate Source: ASM America, Phoenix, AZ, USA
Conference Title: Proceedings of the 1999 MRS Spring Meeting - Symposium on Ultrathin SiO2 and High-k Materials for ULSI Gate Dielectrics
Conference Location: San Francisco, CA, USA Conference Date: 19990405-19990408
E.I. Conference No.: 55914
Source: Materials Research Society Symposium - Proceedings v 567 1999. p 147-154
Publication Year: 1999
CODEN: MRSPDH ISSN: 0272-9172
Language: English
Abstract: The MESC/CTMC compatible, Advance 2500 cluster tool made by ASM is evaluated for the manufacturing of CMOS gate stack structures based on CVD **silicon nitride** rather than thermally grown silicon oxide as the gate dielectric material, and polysilicon as the gate electrode material. With two different CVD chemistries excellent growth

characteristics and thickness uniformity control of the **silicon nitride** is demonstrated. Electrical assessment reveals lower leakage current as compared to silicon oxide and minimal hysteresis in C-V curves, even for gates stacks that have an equivalent oxide thickness below 1.5nm. The best properties are for **silicon nitride films** that also have a low H//2 content. (Author abstract) 4 Refs.

24/3,AB/14 (Item 4 from file: 8)
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05378652
E.I. No: EIP99104816862
Title: Silicon oxide/**silicon nitride** dual-**layer** films: A stacked gate dielectric for the 21st century
Author: Lucovsky, Gerald
Corporate Source: North Carolina State Univ, Raleigh, NC, USA
Conference Title: Proceedings of the 1998 2nd International Conference on Amorphous and Crystalline Insulating Thin Films II
Conference Location: Hong Kong, China Conference Date: 19981012-19981014
E.I. Conference No.: 55673
Source: Journal of Non-Crystalline Solids v 254 1999. p 26-37
Publication Year: 1999
CODEN: JNCSBJ ISSN: 0022-3093
Language: English
Abstract: Incorporation of nitrogen atoms into ultra thin (less than 0.3 nm) gate dielectrics (i) reduces defect generation at the Si-SiO//2 interface, (ii) allows use of physically thicker dielectrics when incorporated into oxide-nitride stacked gate dielectrics, and (iii) prevents boron atom transport out of heavily doped p** plus polycrystalline silicon gate electrodes when nitrided layers are incorporated at the polycrystalline Si-dielectric interface. I demonstrate that nitrogen atoms can be selectively and independently incorporated into different parts of the gate dielectric structure by low-temperature (approximately 300 degree C) remote plasma assisted processing followed by low-thermal budget rapid thermal annealing (RTA) yielding state of the art field effect transistors with oxide equivalent thicknesses less than 2 nm. (Author abstract) 24 Refs.

24/3,AB/15 (Item 5 from file: 8)
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05110037
E.I. No: EIP98094359932
Title: Hydrogen/deuterium interaction with CMOS **transistor** device structure: Sintering process studied by SIMS
Author: Chen, P.J.; Wallace, R.M.
Corporate Source: Texas Instruments Inc, Dallas, TX, USA
Conference Title: Proceedings of the 1998 MRS Spring Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19980413-19980417
E.I. Conference No.: 48894
Source: Hydrogen in Semiconductors and Metals Materials Research Society Symposium Proceedings v 513 1998. MRS, Warrendale, PA, USA. p 325-330
Publication Year: 1998
CODEN: MRSPDH ISSN: 0272-9172
Language: English

Abstract: Passivation of the SiO//2-Si interface by hydrogen/deuterium in MOS transistors serve to ensure their operating reliability against channel hot carriers. Physical characterization of device sintering process in deuterated forming gas (10%D//2:90%N//2) is carried out by dynamic SIMS on planar CMOS gate stack structures, in conjunction with device hot carrier electrical testing. It is found that incorporation of deuterium in the doped poly-Si/SiO//2/Si interfacial region readily occurs under typical post-metallization sintering conditions, demonstrating that transport of deuterium through CMOS gate is an effective pathway in an **encapsulated** device structure with **silicon nitride** sidewalls. The measured Si-D areal densities in the interfacial region depend on gate poly-Si doping type, but in both cases, appear to be sufficient to achieve complete interface Si dangling bond (approximately 10**1**2 cm** minus **2) passivation for the SiO//2-Si system. (Author abstract) 10 Refs.

24/3,AB/16 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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04464707
E.I. No: EIP96083273060
Title: Advanced ion implantation and rapid thermal annealing technologies for highly reliable 0.25 mu m dual gate CMOS
Author: Shimizu, S.; Kuroi, T.; Kawasaki, Y.; Tsutsumi, T.; Oda, H.; Inuishi, M.; Miyoshi, H.
Corporate Source: Mitsubishi Electric Corp, Hyogo, Jpn
Conference Title: Proceedings of the 1996 Symposium on VLSI Technology
Conference Location: Honolulu, HI, USA Conference Date: 19960611-19960613
E.I. Conference No.: 45102
Source: Digest of Technical Papers - Symposium on VLSI Technology 1996. IEEE, Piscataway, NJ, USA,96CH35944. p 64-65
Publication Year: 1996
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: Advanced ion implantation and rapid thermal annealing technologies are proposed to realize highly reliable 0.25 mu m salicided dual gate CMOS for high performance logic application. These technologies mainly consist of mixing the CoSi//2/Si interface using silicon implantation, CVD-Si//3N//4/CVD-SiO//2 sidewall spacer, nitrogen implantation in gate polysilicon and **source/drain** regions and rapid thermal annealing (RTA) for reduction of thermal budget. (Author abstract) 4 Refs.

24/3,AB/17 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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03322463
E.I. Monthly No: EIM9110-053907
Title: An In//0//.//5//3Ga//0//.//4//7As embedded PIN photodiode and an In//0//.//5//3Ga//0//.//4//7As voltage-tunable transimpedance amplifier.
Author: Lo, D. C. W.; Chung, Y. K.; Forrest, S. R.
Corporate Source: Dept of Electr Eng & Mater Sci, Univ of Southern California, Los Angeles, CA, USA
Conference Title: LEOS Summer Topical on Integrated Optoelectronics
Conference Location: Monterey, CA, USA Conference Date: 19900730
E.I. Conference No.: 15150

12/04/2002

Source: LEOS Summer Top Integr Optoelectron. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90TH0321-0). p 74-75
Publication Year: 1990
Language: English
Abstract: A narrow-gate In//0//.//5//3Ga//0//.//4//7As JFET (5 mu m wide and 30 mu m long) is used as an active feedback resistor for the transimpedance amplifier. In addition to the active resistors, the transimpedance amplifier has a common **source** inverter stage and a level-shift buffer stage. The output resistance of the narrow-gate **transistor** operated in its linear region can be dynamically tuned over a wide range. The device can be made very small to reduce parasitic capacitance and inductance. The embedded PIN diode was fabricated on an unintentionally doped In//0//.//5//3Ga//0//.//4//7As layer grown by LPE in a 4- mu m-deep, 250- mu m-wide stripe etched into the SI-InP substrate. The amplifiers were fabricated on a 0.7- mu m-thick n-type (5 multiplied by 10**1**6cm**-**3) In//0//.//5//3Ga//0//.//4//7As layer grown outside of the stripes. The electronic device active region was isolated by mesa etching down to the substrate. Zn from a ZnAs//2 **source** was selectively diffused in a sealed **quartz** ampoule at 520 degree C to form the p-n junction. After p-contact metal (Cr-Au) was deposited, the **SiN**//x diffusion mask was removed, and a crystallographically selective etchant was used to undercut the metal gate and thereby reduce p-n junction parasitic sidewall capacitance. Cr-Au was deposited to form the n-contact. The integrated receiver has a **chip** size of only 0.4 mm multiplied by 0.9 mm. 2 Refs.

24/3,AB/18 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

10313523 Genuine Article#: 509PY Number of References: 40
Title: Ultrathin zirconium oxide films as alternative gate dielectrics (ABSTRACT AVAILABLE)
Author(s): Chang JP (REPRINT) ; Lin YS; Berger S; Kepten A; Bloom R; Levy S
Corporate Source: Univ Calif Los Angeles,Dept Chem Engn,Los Angeles//CA/90095 (REPRINT); Univ Calif Los Angeles,Dept Chem Engn,Los Angeles//CA/90095; Technion Univ,Dept Mat Engn,IL-32000 Haifa//Israel/; Mattson Technol Inc,Fremont//CA/94538
Journal: JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B, 2001, V19, N6 (NOV-DEC) , P2137-2143
ISSN: 1071-1023 Publication date: 20011100
Publisher: AMER INST PHYSICS, CIRCULATION & FULFILLMENT DIV, 2 HUNTINGTON QUADRANGLE, STE 1 N O 1, MELVILLE, NY 11747-4501 USA
Language: English Document Type: ARTICLE
Abstract: ZrO2 films were deposited on Si(100) **wafers** by the rapid thermal chemical vapor deposition process using a zirconium (IV) t-butoxide Zr(OC4H9)(4) Precursor and oxygen. Interfacial zirconium silicate formation was observed by high resolution transmission electron microscopy and medium energy ion scattering. The intermixing of the interface can be suppressed by forming a thin **silicon nitride layer** on the **silicon** substrate prior to ZrO2 deposition. The dielectric constant of ZrO2 achieved in this work is 15-18 with very small capacitance-voltage hysteresis, ideal for metal-oxide-semiconductor field effect **transistor** (MOSFET) application. The NMOSFET device has good turn-on characteristics, however, the transconductance is lower than expected due to the incomplete removal of zirconium silicate at the **source** and **drain** contacts and poses integration challenges to use ZrO2 as the gate dielectric material. (C) 2001 American Vacuum Society.

12/04/2002

24/3,AB/19 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

06098396 Genuine Article#: XU851 Number of References: 4
Title: Shallow trench isolation for sub-0.25-mu m **IC** technologies (ABSTRACT AVAILABLE)
Author(s): Nag S (REPRINT) ; Chatterjee A
Corporate Source: TEXAS INSTRUMENTS INC,CTR SEMICOND PROC & DEVICE, 13570 N CENT EXPRESSWAY, MS 3701/DALLAS//TX/75243 (REPRINT)
Journal: SOLID STATE TECHNOLOGY, 1997, V40, N9 (SEP), P129-&
ISSN: 0038-111X Publication date: 19970900
Publisher: PENNWELL PUBL CO SOLID STATE TECHNOLOGY OFFICE, TEN TARA BLVD 5TH FLOOR, NASHUA, NH 03062-2801
Language: English Document Type: ARTICLE
Abstract: Transistors in **ICs** have conventionally been isolated by growing thick **SiO2** thermally in the regions between them, This so-called local oxidation of silicon (LOGOS) masks off the active areas with a **layer** of **silicon nitride** (Fig. 1a). The main drawback of LOCOS, the unacceptably large dimension of the ''bird's beak,'' limits its utility for the smaller geometries in sub-0.25-mu m designs. Shallow trench isolation (STI), in contrast, uses deposited dielectrics to fill trenches etched in the silicon between the active areas, In principle, it is only limited by the lithography, etch, and gap-fill depositions, which have thus far scaled with **transistor** technology. Therefore, STI is an attractive alternative to LOCOS for deep submicron **ICs**. This article discusses key considerations in the development of the STI module and highlights potential problems for large-scale implementation of STI in **wafer** fabrication.

24/3,AB/20 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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04166900 Genuine Article#: RK195 Number of References: 13
Title: ROOM-TEMPERATURE DEPOSITION OF SINX USING ECR-PECVD FOR III/V SEMICONDUCTOR **MICROELECTRONICS** IN LIFT-OFF TECHNIQUE (Abstract Available)
Author(s): WIERSCH A; HEEDT C; SCHNEIDERS S; TILDERS R; BUCHALI F; KUEBART W; PROST W; TEGUDE FJ
Corporate Source: GERHARD MERCATOR UNIV,DEPT SOLID STATE ELECTR,SONDERFORSCHUNGSBEREICH 254,KOMMANDANTENSTR 60/D-47057 DUISBURG//GERMANY/; GERHARD MERCATOR UNIV,DEPT SOLID STATE ELECTR/D-47057 DUISBURG//GERMANY/; ALCATEL SEL/STUTTGART//GERMANY/
Journal: JOURNAL OF NON-CRYSTALLINE SOLIDS, 1995, V187, JUL (JUL), P334-339
ISSN: 0022-3093
Language: ENGLISH Document Type: ARTICLE
Abstract: Room-temperature deposition of **silicon-nitride** on InP-substrates for electronic applications is reported. A plasma enhanced chemical vapour deposition apparatus equipped with an electron cyclotron resonance **source** was used. Molecular nitrogen and silane diluted in helium are chosen as precursors. The dielectric films are defined by means of optical lithography and lift-off technique. C-f measurements reveal a dielectric constant of about 9 and a dissipation factor tan delta = 3 x 10(-1) (f = 10 kHz) while the breakdown field is 2 MV/cm (I = 250 mu A/mm(2)). A strong improvement of the dissipation factor by more than one order of magnitude under both electrical and thermal stress, respectively, has been observed which could not be related to a variation of Si-H or N-H bonds measured by Fourier

transformed infrared spectroscopy. The influence of **silicon-nitride** deposition on the electrical properties of an InAlAs/InGaAs heterostructure field-effect **transistor** is investigated. The most significant change is found as an improvement of gate leakage current by 90% while other dc- and rf-properties remain unchanged.

24/3,AB/21 (Item 4 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

03974777 Genuine Article#: QW861 Number of References: 29
Title: ROOM-TEMPERATURE, HIGH-DEPOSITION-RATE, PLASMA-ENHANCED CHEMICAL-VAPOR-DEPOSITION OF **SILICON** OXYNITRIDE THIN-**FILMS** PRODUCING LOW SURFACE DAMAGE ON LATTICE-MATCHED AND PSEUDOMORPHIC III-V QUANTUM-WELL STRUCTURES (Abstract Available)
Author(s): SAH RE; RALSTON JD; EICHIN G; DISCHLER B; ROTHEMUND W; WAGNER J; LARKINS EC; BAUMANN H
Corporate Source: FRAUNHOFER INST ANGEW FESTKORPER PHYS,TULLASTR 72/D-79108 FREIBURG//GERMANY/; UNIV FRANKFURT,INST KERNPHYS/D-60486 FRANKFURT//GERMANY/
Journal: THIN SOLID FILMS, 1995, V259, N2 (APR 15), P225-230
ISSN: 0040-6090
Language: ENGLISH Document Type: ARTICLE
Abstract: **Silicon** oxynitride thin **films** have been deposited at room temperature on GaAs using the PECVD technique with SiH4, N2O and Ar in a modified magnetron sputtering system. Typical deposition rates were on the order of 350 nm min(-1), substantially higher than has been previously achieved for room-temperature deposition with good optical and mechanical quality. At a fixed ratio of precursor gases SiH4:N2O:Ar = 14:33:160 sccm, bias potential V-B = - 50 V, and total deposition pressure P = 32 mTorr, the atomic ratios of Si/O and N/O were found to be 1.25 and 0.14, respectively, using Rutherford backscattering spectroscopy. From nuclear reaction analysis, the hydrogen content was found to be 6 at.%, much lower than is typical for low-temperature PECVD films. The deviation in the uniformity of the film thickness was within +/- 4% across a 2'' GaAs **wafer**. For the above deposition conditions, the refractive index and the optical band-gap of the films were 1.9 and 2.0 eV, respectively. Raman and photoluminescence spectra show practically no surface damage following film deposition on GaAs/AlGaAs modulation-doped field-effect **transistor**, unstrained GaAs/AlGaAs quantum-well (QW) structures and pseudomorphic InGaAs/GaAs QW structures.

24/3,AB/22 (Item 5 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

03096989 Genuine Article#: NA072 Number of References: 11
Title: DEVELOPMENT OF MOS-TRANSISTORS FOR RADIATION-HARDENED LARGE-SCALE **INTEGRATED-CIRCUITS** AND ANALYSIS OF RADIATION-INDUCED DEGRADATION (Abstract Available)
Author(s): KAMIMURA H; YOSHIOKA S; AKIYAMA M; NAKAMURA M; TAMURA T; KUBOYAMA S
Corporate Source: HITACHI LTD,ENERGY RES LAB,OMIKA CHO/HITACHI 31912//JAPAN/; HITACHI LTD,CTR SEMICOND DESIGN & DEV/KODAIRA 187//JAPAN/; HITACHI LTD,DIV SPACE SYST,CHIYODA KU/TOKYO 101//JAPAN/; NATL SPACE DEV AGCY JAPAN,TSUKUBA SPACE CTR/TSUKUBA 305//JAPAN/; NATL SPACE DEV AGCY JAPAN,DEPT RELIABIL ASSURANCE,MINATO KU/TOKYO

12/04/2002

105//JAPAN/
Journal: JOURNAL OF NUCLEAR SCIENCE AND TECHNOLOGY, 1994, V31, N1 (JAN), P 24-33
ISSN: 0022-3131
Language: ENGLISH Document Type: ARTICLE
Abstract: Radiation-hardened MOSFETs were developed. and experimental results on their total dose degradation were collected to evaluate effects of three techniques for radiation hardening. The three techniques are; (1) adding a **silicon-nitride layer** onto the phospho-silicate glass passivation layer, (2) thinning of the field oxide by increasing resistance of the channel stopper, and (3) annealing the gate oxide at lower temperature. Technique (1) suppressed the leakage current generated by the parasitic MOSFET, because the negative threshold voltage shift of the parasitic MOSFET was compensated by the positive shift due to the interface states generated by hydrogen trapped in the oxide by the **silicon nitride** deposition. Furthermore, leakage current decreased with technique (2) as well. Technique (3) was not effective because the gate oxide is inherently thin. Results gotten using a linear model for the threshold voltage shift represented well the measured data up to 1.5 kGy(Si) at a dose rate of 5 Gy(Si)/h.

24/3,AB/23 (Item 6 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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02010741 Genuine Article#: JU285 Number of References: 156
Title: INTEGRATED PROCESSING FOR **MICROELECTRONICS** SCIENCE AND TECHNOLOGY (Abstract Available)
Author(s): RUBLOFF GW; BORDONARO DT
Corporate Source: IBM CORP,THOMAS J WATSON RES CTR,DIV RES,POB 218/YORKTOWN HTS//NY/10598; IBM CORP,TECHNOL PROD,BURLINGTON FACIL/ESSEX JCT//VT/05452
Journal: IBM JOURNAL OF RESEARCH AND DEVELOPMENT, 1992, V36, N2 (MAR), P 233-276
ISSN: 0018-8646
Language: ENGLISH Document Type: REVIEW
Abstract: This paper is a review of integrated processing-an approach to **microelectronics** fabrication in which sequential processes are linked by **wafer** transfer through a clean, controlled environment (e.g., high vacuum or inert gas). The approach is rapidly becoming the state of the art in **microelectronics** research, development, and manufacturing. In **microelectronics** research, it provides a means for advancing mechanistic understanding and material quality through in situ fabrication of test structures and extensive in situ diagnostics. In **microelectronics** development and manufacturing, it promises process simplification, improved contamination control and yield, and potentially more flexible equipment utilization. With increasing emphasis on ultraclean processing, involving control of reactive impurities as well as particles, and on real-time process monitoring and control, applications of integrated processing are moving toward a common ground in which state-of-the-art research techniques can be used to address key issues in development and manufacturing, and provide in return substantive guidelines for manufacturing design and practice.

24/3,AB/24 (Item 7 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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12/04/2002

01223961 Genuine Article#: GF539 Number of References: 276
Title: STRESS-RELATED PROBLEMS IN SILICON TECHNOLOGY (Abstract Available)
Author(s): HU SM
Corporate Source: IBM CORP,DIV GEN TECHNOL/HOPEWELL JUNCTION//NY/12533
Journal: JOURNAL OF APPLIED PHYSICS, 1991, V70, N6, PR53-R80
Language: ENGLISH Document Type: REVIEW

Abstract: The silicon **integrated-circuits chip** is built by contiguously embedding, butting, and overlaying structural elements of a large vaiety of materials of different elastic and thermal properties. Stress develops im the thermal cycling of the **chip**. Furthermore, many structural elements such as CVD (chemical vapor deposition) **silicon nitride, silicon dioxide,** polycrystalline silicon, etc., by virture of their formation proceses, exhibit intrinsic stresses. Large localized stresses are induced in the silicon substrate near the edges and corners of such structural elements. Oxidation of nonplanar silicon surfaces produces another kind of stress that can be very damaging, especially at low oxidation temperatures.

Mismatch of atomic sizes between dopants and the silicon, and heteroepitaxy produce another class of strain that can lead to the formation of misfit dislocations. Here we review the achievements to date in understanding and modeling these diverse stress problems.

24/3,AB/25 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
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01094048 AAD9008089
CHARACTERIZATION AND MODELING OF CHARGE TRAPPING AND RETENTION IN NOVEL MULTI-DIELECTRIC NONVOLATILE SEMICONDUCTOR MEMORY DEVICES

Author: ROY, ANIRBAN
Degree: PH.D.
Year: 1989
Corporate Source/Institution: LEHIGH UNIVERSITY (0105)
Source: VOLUME 50/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 4695. 249 PAGES

This dissertation deals with the synthesis and analysis of new multidielectric memory devices to identify a viable low voltage programmable (5-10V) electrically erasable programmable read only memory (EEPROM) cell for memory densities exceeding 1MB/**chip**. The memory devices are variations of the triple dielectric **silicon dioxide -silicon nitride-silicon dioxide** (ONO) structure, where the **silicon nitride** is the "memory layer". We have developed physically based analytical and numerical models to explain the charge trapping and storage in the scaled down nitride ($\sim$100 A) layer. The recombination kinetics in the nitride is modeled with amphoteric traps acting as "memory" centers for electrons and holes injected through the tunneling oxide during programming.

We have investigated electron and hole charge separation at the silicon-insulator interface. Surface channel or **buried** channel transistors can only separate electrons and holes under one gate bias polarity. We have demonstrated, for the first time, charge separation for both gate polarities with the specially designed dual channel (n-**buried** channel and p-surface channel under the same gate) **transistor**. We have gained evidence to prove that the memory properties of thin-oxide SONOS devices is dominated by electron and hole recombination in the nitride bulk.

We have fabricated ONO memory capacitors and transistors with

bottom(tunneling) oxide thicknesses in the range of 15-23A, nitride thicknesses in the range of 50-205A and top(blocking) oxide thicknesses in the range of 17-56A. We have demonstrated 5-10V programming on both uniform and graded(Si-rich composition bounded by N-rich composition) nitride ONO memory devices. We have shown that the graded nitride devices are better than uniform composition nitride for long term ($>$10 years) charge retention. We have shown that a Au gate electrode reduces electron injection from the gate for large negative gate bias, when compared with Al or n$\sp+$ poly gate electrodes. Based on this research, we recommend a SONOS memory **transistor** with a 20A SiO$\sb2$/45A N-rich Si$\sb3$N$\sb4$/40A Si-rich Si$\sb3$N$\sb4$/25A LPCVD SiO$\sb2$/25A steam-oxidized SiO$\sb2$ dielectric stack and p$\sp+$-poly gate for 5-10V programmability and greater than 10 years charge retention.

24/3,AB/26 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
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918710 AAD8612772
THERMAL AND PLASMA NITRIDATION OF SILICON AND **SILICON DIOXIDE** FOR ULTRATHIN GATE INSULATORS OF MOS VLSI
Author: MOSLEHI, MEHRDAD MAHMUD
Degree: PH.D.
Year: 1986
Corporate Source/Institution: STANFORD UNIVERSITY (0212)
Source: VOLUME 47/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 1203. 408 PAGES

The down-scaling of metal-oxide-semiconductor devices motivated by the continuing increase in the integration density of **integrated circuits** requires a substantial reduction in oxide thickness in the field-effect **transistor** gate, dynamic random-access memory storage capacitor, and nonvolatile-memory tunnel dielectrics. The technological and reliability problems associated with **silicon dioxide** (oxide) in the very thin regime emphasize the need for alternative high-quality insulators and new growth techniques. **Silicon nitride,** nitrided oxide (nitroxide), and oxidized nitride (oxynitride) grown by thermal and plasma nitridations are proposed as the best available alternatives. The new techniques include thermal nitridation in a lamp-heated system, and low-temperature microwave nitrogen-plasma nitridation.

Knowledge of the growth kinetics and electrical characteristics of thin oxide is essential for the development of new dielectrics formed by subsequent processing of an initially grown oxide.

The kinetics of the thermal nitridation of silicon and **silicon dioxide** in an ammonia ambient are analyzed. The electrical characteristics of metal-insulator-semiconductor devices with thermal **silicon-nitride** and nitroxide gate dielectrics are examined, and the results indicate the excellent electrical stability of the **silicon-nitride** devices because of very low carrier trapping. The interface transition from nitride to silicon is abrupt, and the morphology and roughness of the interface are comparable to the oxide/silicon interfaces.

Rapid thermal nitridation is a possible approach to the use of higher temperatures for very short times. Application of this process to **silicon dioxide** creates nitrided barrier layers at the surface and interface, increases interfacial charge densities, and slows the generation rate of new surface states resulting from electrical stress. The formation kinetics of these nitrogen-rich layers are correlated to the electrical behavior of the rapidly grown nitroxides.

A new plasma-nitridation technique based on nitrogen plasma

generated by microwave discharge reduces nitridation temperature and enhances the growth kinetics. From grazing-angle Rutherford backscattering data, these **silicon-nitride films** (30 to 100 (ANGSTROM)) have some oxygen and carbon contamination but exhibit good breakdown characteristics under optimal plasma and growth conditions.

24/3,AB/27 (Item 3 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
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833705 AAD8402296
A MONOLITHIC PH/PRESSURE/TEMPERATURE SENSOR FOR ESOPHAGEAL STUDIES
Author: HUANG, (JAMMY) CHIN-MING
Degree: PH.D.
Year: 1983
Corporate Source/Institution: THE UNIVERSITY OF MICHIGAN (0127)
Source: VOLUME 44/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 3141. 143 PAGES

This study was initiated to apply silicon **integrated circuit** technology to the development of a monitoring system for esophageal studies. A monolithic composite sensor consisting of a capacitive pressure transducer and an ion (pH) sensitive field effect **transistor** (ISFET) was designed, fabricated, and tested together with custom interface electronics. This sensor can be used to monitor pH and pressure at multiple sites along the esophagus in ambulatory patients.

The thin diaphragm of the capacitive pressure sensor was fabricated using the boron etch-stop technique to achieve precise thickness control (from a few tenths of a micron to about 20 microns) in a batch process. An electro-static sealing process was utilized to simultaneously form an anodic glass-to-silicon bond as well as a thermocompression bond for lead transfer between the glass electrode and the on-**chip** electronics.

The lead access between the exposed ISFET and the **encapsulated** on-**chip** electronics on the reverse side of the **wafer** was achieved by an anisotropic etching technique. This technique allows all of the leads to be accessed from a single side of the **wafer** and greatly simplifies the packaging of the completed sensor.

A temperature model for the ISFET is derived by introducing an effective work function for the electrolyte/reference electrode system. This model is then exploited to minimize the temperature sensitivity of the ISFET. The ISFET, which utilizes a 100 nm-thick **silicon nitride** gate dielectric over 100 nm of **silicon dioxide**, achieves a pH sensitivity of typically 50 mV/pH with a temperature coefficient equivalent to 15 mpH/(DEGREES)C. The capacitive pressure transducer has a pressure sensitivity of 1000 ppm/mmHg and a temperature sensitivity of about +30 ppm/(DEGREES)C. Since the temperature coefficients are sufficiently low, no individual compensation for temperature is needed over the 10 - 40(DEGREES)C range encountered in the esophagus.

The on-**chip** signal processing electronics were designed and implemented using an n-MOS all-enhancement-mode silicon-gate LOCOS process. Schmitt trigger and bootstrap techniques were used to modify a three-stage ring oscillator and achieve high capacitance sensitivity (300 KHz/pF on a 1.6 MHz carrier) in the range from 1pF to 5pF. The relatively high temperature sensitivity of the circuitry (1.7 KHz/(DEGREES)C) can be utilized as a temperature sensor in the esophageal monitoring system; however, the oscillator is used to alternately pass the pressure signal and a pressure-independent reference so that temperature drift in the pressure offset signal can be eliminated externally. The complete pressure-pH sensor

is compatible with use in a four-site single-lumen catheter having a diameter of 3 mm.

24/3,AB/28 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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04845148 JICST ACCESSION NUMBER: 01A0200948 FILE SEGMENT: JICST-E
Effects of Backgate Voltage on Electrical Characteristics of Poly-**Si** Thin **Film** Transistors Fabricated on Stainless-Steel Substrate.
SERIKAWA T (1); OMATA F (1)
(1) Ntt Cyber Space Lab., Tokyo, Jpn
Jpn J Appl Phys Part 2, 2000, VOL.39,NO.12B, PAGE.L1277-L1279, FIG.3, REF.9
JOURNAL NUMBER: F0599BAD ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382 MIS 621.382.3
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: High mobility p-channel polycrystalline **Si** thin **film** transistors(poly-**Si** TFTs) are fabricated on flexible stainless-steel substrates coated with 500-nm-thick **SiO2** and 50-nm-thick **SiN** films. The electrical characteristics of mobility, threshold voltage and subthreshold slope are first measured at a function of backgate voltage VBG of from -26V to +20V applied on stainless-steel substrate. Mobilities show small dependence on VBG. Threshold voltages, however, have dependence of decreasing with increasing VBG. Subthreshold slopes also show concave-shaped dependence on VBG. The results indicate that electrical characteristics of poly-Si TFTs are controlled by simply applying voltages to the substrate. Thus, application of backgate voltage are very important for design advanced poly-Si TFT **integrated circuits** and to secure stable operation of the circuits. (author abst.)

24/3,AB/29 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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04782934 JICST ACCESSION NUMBER: 01A0171757 FILE SEGMENT: JICST-E
High Performance CMOS Technology for Large Scale System-on-a-**chip** in 130-nm Node.
ONAI TAKAHIRO (1); ONISHI KAZUHIRO (1); OTSUKA FUMIO (1)
(1) Hitachi, Ltd.
Handotai, Shuseki Kairo Gijutsu Shinpojiumu Koen Ronbunshu(Proceedings of the Symposium on Semiconductors and Integrated Circuits Technology), 2000, VOL.59th, PAGE.12-17, FIG.11, TBL.1, REF.6
JOURNAL NUMBER: F0108BAP
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A 0.1-.MU.m CMOS technology for high-speed SoC(System-on-a-**Chip**) and microprocessors has been successfully achieved. The **transistor** has an SiO/**SiN** stacked gate dielectric with Tox(inv)=2.8nm(EOT=2.0nm) to avoid gate direct tunneling leakage and boron penetration. The gate leakage current was reduced by one order of magnitude compared to **SiO2**. This **transistor** also utilizes a

polySi/metal stacked gate electrode to reduce gate resistance. This gate stack structure enables self-align contacts against the gate electrode and damascene local interconnect over the gate electrode, which minimize the 6T-SRAM cell size down to 2.3.MU.m2. Careful design of the **source/drain** layers offers good short channel operation below 0.1-.MU.m gate length and high drive currents of 1000.MU.A/.MU.m for a NMOS and 410.MU.A/.MU.m for a PMOS at a 1.5V voltage supply. From the analysis using BSIM3 model, it was found that reducing the resistance of the **source/drain** extensions could increase the drive current of PMOS. The **transistor** has sufficiently long lifetime for hot carrier effect. (author abst.)

24/3,AB/30   (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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04410981   JICST ACCESSION NUMBER: 00A0014475 FILE SEGMENT: JICST-E
Anomalous Junction Leakage Current Induced by Plasma Dry Etch of Shallow Trench Isolation(STI).
LINLIU K (1); WU K H (1); LIN H C (1); CHANG K H (1); LIN J (1); JENG S P (1); CHI M H (1)
(1) Worldwide Semiconductor Manufacturing Corp.(wsmc), Taiwan
Proc Symp Dry Process, 1999, VOL.21st, PAGE.149-154, FIG.12, TBL.1, REF.17
JOURNAL NUMBER: Y0378AAE
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2   533.9.06
LANGUAGE: English   COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: An anomalous junction leakage current induced by the plasma dry etch of shallow trench isolation(STI) was investigated. The anomalous junction leakage current occurs when the silicon sidewall in the shallow trench is rough. This phenomenon limits the minimal dimension for the isolation in active area. Even when the isolation space of STI is smaller than 0.22.MU.m, if the surface is smooth, the junction leakage is negligible. For the **silicon nitride** etch, when the gas ratio of CF4 over CHF3 is smaller than 1, the angle of **silicon nitride** profile is around 80.DEG.-84.DEG., and the **silicon nitride** sidewall is very rough. This roughness is later transferred to the sidewall of silicon. We developed an optimized plasma dry etch process to improve the roughness of silicon sidewall and the anomalous junction leakage current. A gas mixture of O2, CF4 and CHF3 is used for **silicon nitride** etching. When the gas ratio of CF4/CHF3 is greater than 1.5, the **silicon nitride** profile is larger than 87.DEG., and a smooth **silicon nitride** sidewall and silicon substrate is obtained. The anomalous junction leakage current is also eliminated. In this study, two kinds of dielectric **silicon dioxide films** HDP CVD and SACVD are used for shallow trench gap filling to inquire into the impact on junction leakage current of STI. The junction leakage current of HDP CVD filled STI generally is higher than that of SACVD at the various measured temperature 25.DEG.C., 85.DEG.C. and 125.DEG.C. in STI process. (author abst.)

24/3,AB/31   (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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04277398   JICST ACCESSION NUMBER: 99A0497735 FILE SEGMENT: JICST-E

12/04/2002

Facet-Free Si Selective Epitaxial Growth Adaptable to Elevated **Source** **/Drain** MOSFETs with Narrow Shallow Taench Isolation.
MIYANO K (1); MIZUSHIMA I (1); OHUCHI K (1); HOKAZONO A (1); TSUNASHIMA Y (1)
(1) Toshiba Corp., Yokohama, Jpn
Jpn J Appl Phys Part 1, 1999, VOL.38,NO.4B, PAGE.2419-2423, FIG.14, REF.6
JOURNAL NUMBER: G0520BAE   ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2   621.382.3
LANGUAGE: English   COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A novel selective epitaxial growth (SEG) process that realizes a facet-free elevated **source/drain** (S/D) is proposed. The key points are the appropriate selection of the gate-sidewall material and its structural improvement. It was observed that the facet was not formed adjacent to **SiN** in contrast to the **SiO2** case. Therefore, **SiN** is selected as a gate-sidewall. The novel gate,-side,wall is constructed from a **SiN** sidewall and **SiO2** liner layer which acts as a sidewall reactive ion etching (RIE) stopper. The **SiO2** liner layer is lateral etched by wet treatment. By the SEG process, the facet, which is formed adjacent to the **SiO2** liner is screened out within the lateral etched region, and no facet is observed along the **SiN** sidewall. Si lateral overgrowth on the shallow trench isolation (STI) region was also confirmed to be controllable in the facet-free SEG process. This novel SEG process was found to be successfully adapted to facet-free elevated S/D. (author abst.)

24/3,AB/32   (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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04250412   JICST ACCESSION NUMBER: 99A0609727 FILE SEGMENT: JICST-E
Highly Integrated Single Electron Devices and Giga-bit Lithograpy.
HIRAMOTO T (1); ISHIKURO H (1); MAJIMA H (1)
(1) Univ. Tokyo, Tokyo, Jpn
J Photopolym Sci Technol, 1999, VOL.12,NO.3, PAGE.417-422, FIG.14, REF.13
JOURNAL NUMBER: L0202AAN   ISSN NO: 0914-9244   CODEN: JSTEE
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77   537.533/.534.06
LANGUAGE: English   COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Single electron transistors and memories for VLSI applications are fabricated and their characteristics are intensively investigated. It is shown that single electron transistors operating at room temperature are affected by quantum confinement effects and are very sensitive to the device size. Single electron memories with narrow channel MOSFETs also have large characteristics fluctuations. These results indicate that high resolution lithography with very high accuracy is strongly required for future giga-bit level single electron devices. MOSFETs with very narrow channel are also fabricated by electron-beam lithography, and the dependence of size fluctuations and **drain** current fluctuations on resist material is examined. (author abst.)

24/3,AB/33   (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

12/04/2002

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1554662 H.W. WILSON RECORD NUMBER: BAST97061592
Shallow trench isolation for sub-0.25-mm **IC** technologies
Nag, Somnath; Chatterjee, Amitava
Solid State Technology v. 40 (Sept. '97) p. 129-30+
DOCUMENT TYPE: Feature Article ISSN: 0038-111X

ABSTRACT: Transistors in **ICs** have conventionally been isolated by growing thick **SiO2** thermally in the regions between them. This so-called local oxidation of silicon (LOCOS) masks off the active areas with a **layer** of **silicon nitride** (Fig. 1a). The main drawback of LOCOS, the unacceptably large dimension of the "bird's beak," limits its utility for the smaller geometries in sub-0.25-mm designs. Shallow trench isolation (STI), in contrast, uses deposited dielectrics to fill trenches etched in the silicon between the active areas. In principle, it is only limited by the lithography, etch, and gap-fill depositions, which have thus far scaled with **transistor** technology. Therefore, STI is an attractive alternative to LOCOS for deep submicron **ICs**. This article discusses key considerations in the development of the STI module and highlights potential problems for large-scale implementation of STI in **wafer** fabrication. Reprinted with the permission of Solid State Technology.

24/3,AB/34 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
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14797038 PASCAL No.: 00-0477429
Silicon oxide and **silicon nitride** thin **film** deposition using RF magnetron sputtering
Physics of semiconductor devices : Delhi, 14-18 December 1999
KUMAR M; AHMAD S; GEORGE P J; YADAV M S
VIKRAM KUMAR, ed; AGARWAL SK, ed
Central Electronics Engineering Research Institute, Pilani-333 031, India ; Electronic Science Department, Kurukshetra University, Kurukshetra-136 119, India
International Society for Optical Engineering, Bellingham WA, United States
International workshop on the physics of semiconductor devices, 10 (Delhi IND) 1999-12-14
Journal: SPIE proceedings series, 2000, 3975 (p.1) 857-859
Language: English
Silicon oxide and **silicon nitride** are the materials widely used as passivation layer in **integrated circuits** and mask for multilayer lithography. These layers are also used as interlevel dielectrics for metallization structure. Device quality **silicon dioxide** can easily be grown by well known techniques of native oxidation. **Silicon nitride** can also be grown by CVD These techniques involve high temperature process during the growth. In certain cases high temperature processes can not be used specially in compound semiconductor devices fabncation and in amorphous thin film transistors. For such applications we have tried to deposit silicon oxide and **silicon nitride** thin **films** using RF magnetron sputtering at room temperature. Initial studies have shown that the quality of such films are not as good as that grown by conventional techniques. These are good enough to work as a masking layer in the fabrication of devices where low temperature process is required. The optimum process parameters to achieve reasonably uniform thin films with minimum defects has been obtained and the results are presented in this paper.

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24/3,AB/35 (Item 2 from file: 144)
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13195510 PASCAL No.: 97-0459786
Gate dielectric properties of **silicon nitride films** formed by jet vapor deposition

MA T P
HATTORI Takeo, ed; WADA Kazuhiko, ed; HIRAKI Akio, ed
Center for Microelectronic Materials and Structures, and Department of Electrical Engineering, Yale University, New Haven, CT 06520-8284, United States
Musashi Institute of Technology, Setagaya-ku, Tokyo 158, Japan; NTT LSI Laboratories, Atsugi, Kanagawa 243-01, Japan; Department of Electrical Engineering, Osaka University, Suita 565, Japan

ISCSI-2: International Symposium on the Control of Semiconductor Interfaces, 2 (Karuizawa JPN) 1996-10-28
Journal: Applied surface science, 1997, 117-18 259-267
Language: English

High-quality **silicon nitride** (or oxynitride) films made by a novel jet vapor deposition (JVD) technique are described. The JVD process utilizes a high-speed jet of light carrier gas to transport the depositing species onto the substrate to form the desired films. The film composition has been determined to consist primarily of Si and N, with some amounts of O and H. MNS capacitors based on the JVD nitride films deposited directly on Si exhibit relatively low densities of interface traps, fixed charge, and bulk traps. The interface traps at the nitride/Si interface exhibit different properties from those at the SiO SUB 2 /Si interface in several aspects. In contrast to the conventional CVD **silicon nitride**, the high-field I-V characteristics of the JVD **silicon nitride** fit the Fowler-Nordheim tunneling theory over 4-5 orders of magnitude in current, but do not fit at all the Frenkel-Poole transport theory. This is consistent with the much lower concentration of electronic traps in the JVD **silicon nitride**. Results from the carrier separation experiment indicate that electron current dominates the gate current with very little hole contribution. Both theoretical calculation and experimental data indicate that the gate leakage current in JVD **silicon nitride** is significantly lower than that in **silicon dioxide** of the same equivalent oxide thickness. Compared to their MOSFET counterparts, MNS transistors exhibit reduced low-field transconductance but enhanced high-field transconductance, perhaps due to the presence of border traps.

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24/3,AB/36 (Item 3 from file: 144)
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12203367 PASCAL No.: 95-0420078
Effects of package geometry, materials, and **die** design on energy dependence of pMOS dosimeters

BRUCKER G J; KRONENBERG S; GENTNER F
US Army, CECOM, Fort Monmouth NJ, USA

Journal: IEEE transactions on nuclear science, 1995, 42 (1) 33-40
Language: English

This paper presents the results of further studies of dose enhancement in

dual and single-dielectric pMOSFET dosimeters for various package and **die** designs. Eight different MOSFET designs and package types were investigated over a photon energy range from 14 to 1250 keV. Seven X-ray effective energies and two radioactive sources of cesium and cobalt provided the radiation. As in a previous study (1), Rutherford back-scattered electrons were primarily responsible for the dose enhancement factors which achieved values as high as 20. Packages filled with silicon grease, aluminum oxide, or paraffin eliminated the contribution of back-scatter to the enhanced dose. These modifications allowed measurements of the usual dose enhancement at the aluminum or polysilicon gate-**silicon nitride** (dual dielectric devices), or **silicon dioxide** interfaces (single dielectric parts), and at the **silicon nitride-silicon dioxide** interface. In addition to the primary peak in the DEF (Dose Enhancement Factor) curve versus energy at 45.7 keV, there is a second peak at about 215 keV. This peak might be due to enhancements at the interfaces of a MOSFET. These interface effects were small in the single-insulator parts in standard ceramic packages, and significantly larger in the dual-insulator devices. The effects were reduced by filling the packages with the materials as previously described. The geometry of the package, for example, the size of the air gap between the **die**'s surface, and the lid of the package impacts the value of the DEF.

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32/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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7351729 INSPEC Abstract Number: A2002-19-7860F-003, B2002-09-4220-020
Title: Ion implantation of rare earth ions for light emitters
Author(s): Buchal, Ch.; Wang, S.; Lu, F.; Carius, R.; Coffa, S.
Author Affiliation: Inst. fur Schichten und Grenzflachen, Forschungszentrum Julich GmbH, Germany
Journal: Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) Conference Title: Nucl. Instrum. Methods Phys. Res. B, Beam Interact. Mater. At. (Netherlands) vol.190 p.40-6
Publisher: Elsevier,
Publication Date: May 2002 Country of Publication: Netherlands
CODEN: NIMBEU ISSN: 0168-583X
SICI: 0168-583X(200205)190L.40:IREI;1-B
Material Identity Number: G701-2002-011
U.S. Copyright Clearance Center Code: 0168-583X/02/$22.00
Conference Title: Fifteenth International Conference on Ion Beam Analysis (incorporating Twelfth AINSE Conference on Nuclear Techniques of Analysis)
Conference Sponsor: AINSE; Bohmische Phys. Soc.; Elsevier Sci.; High Voltage Eng. Europe; MARCO (Melbourne Univ.); et al
Conference Date: 15-20 July 2001 Conference Location: Cairns, Qld., Australia
Language: English
Abstract: We discuss the excitation and deexcitation processes for solid state optical emitters. At present, there is considerable interest in depositing a material system, which is compatible with Si **microelectronics** processing and which emits electroluminescence (EL). We compare the EL results of rare earth-doped **transistors** in Si with doped insulators and doped wide bandgap semiconductors, especially Er in Si (a **source** for 1.5 mu m) as well as Er and Tb in SiO/sub 2/, Si/sub 3/N/sub 4/ and AlN, which are sources for infrared and visible light. The most impressive results are achieved by RE-doped GaN film devices, which cover the entire visible spectrum.
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32/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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02323309 INSPEC Abstract Number: B84052273
Title: The elimination of devitrification defects in antimony buried-layer diffusions
Author(s): Alvarez, A.R.; Pintchovski, F.
Author Affiliation: Motorola Semiconductor Inc., Mesa, AZ, USA
Journal: Journal of the Electrochemical Society vol.131, no.6 p. 1438-40
Publication Date: June 1984 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
Language: English
Abstract: Doped silicate glasses are widely used as diffusion sources for buried layers in bipolar technology. Thermal oxide is commonly used as a diffusion mask in these processes. More recently, the use of **silicon nitride/silicon dioxide** as a diffusion barrier for this application has been reported. During the diffusion of boron, phosphorus, arsenic, and antimony from doped glass sources, a common type of glass

damage occurs, devitrification, and this damage propagates into the silicon substrate. The authors describe a composite Si/sub 3/Ni/sub 4//SiO/sub 2/ diffusion mask. This mask was found to greatly decrease the levels of devitrification damage induced by antimony diffusions from a doped glass **source** . The reduction in defect density at the buried layer led to improved breakdown characteristics in NPN **transistors** and a concomitant increase in functional circuit yields.
Subfile: B

32/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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00768470 INSPEC Abstract Number: B75019908
Title: Fabrication of small contacts to **source** and **drain** of IGFET's
Author(s): De La Moneda, F.H.
Author Affiliation: IBM, New York, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.17, no.8 p.2361-2
Publication Date: Jan. 1975 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: Describes a method employing **silicon nitride** coatings to mask the growth of a thermal **silicon dioxide** layer in the formation of contact via holes.
Subfile: B

12/04/2002

44/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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7433024 INSPEC Abstract Number: A2002-23-6855-109, B2002-12-2550A-004
Title: New SiC on insulator **wafers** based on the Smart-Cut approach and their potential applications
Author(s): Joly, J.-P.; Aspar, B.; Bruel, M.; Di Cioccio, L.; Letertre, F.; Hugonnard-Bruyere, E.
Author Affiliation: Departement de Microtechnol., Leti CEA, Grenoble, France
Conference Title: Progress in SOI Structures and Devices Operating at Extreme Conditions. Proceedings of the NATO Advanced Research Workshop p.31-8
Editor(s): Balestra, F.; Nazarov, A.; Lysenko, V.S.
Publisher: Kluwer Academic Publishers, Dordrecht, Netherlands
Publication Date: 2002 Country of Publication: Netherlands vii+351 pp.
ISBN: 1 4020 0576 8 Material Identity Number: XX-2002-02693
Conference Title: Progress in SOI Structures and Devices Operating at Extreme Conditions. Proceedings of the NATO Advanced Research Workshop
Conference Date: 15-20 Oct. 2000 Conference Location: Kyiv, Ukraine
Language: English
Abstract: Important progress have been made in the fabrication of SiCOI (Silicon Carbide On Insulator) structures using the Smart-Cut approach. The different structures which have been demonstrated both in terms of transferred layer polytypes (4H and 6H), of handle substrate (silicon or polycrystalline silicon carbide) and of **buried insulator** layers (**silicon dioxide** and **silicon nitride**) are described. Deep traps present in the SiC layer after transfer and annealing of the structure and which are generated by the ion implantation process have been studied using different techniques (Hall measurements, DLTS, photoluminescence, RPE). We see that their density can be strongly minimised making the as transferred layer quality compatible with many applications. Considering both the improved layer quality and the different possible SiCOI structures now available the different possible applications and the perspectives are reviewed.
Subfile: A B
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DIALOG(R)File 2:INSPEC
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7351729 INSPEC Abstract Number: A2002-19-7860F-003, B2002-09-4220-020
Title: Ion implantation of rare earth ions for light emitters
Author(s): Buchal, Ch.; Wang, S.; Lu, F.; Carius, R.; Coffa, S.
Author Affiliation: Inst. fur Schichten und Grenzflachen, Forschungszentrum Julich GmbH, Germany
Journal: Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) Conference Title: Nucl. Instrum. Methods Phys. Res. B, Beam Interact. Mater. At. (Netherlands) vol.190 p.40-6
Publisher: Elsevier,
Publication Date: May 2002 Country of Publication: Netherlands
CODEN: NIMBEU ISSN: 0168-583X
SICI: 0168-583X(200205)190L.40:IREI;1-B
Material Identity Number: G701-2002-011
U.S. Copyright Clearance Center Code: 0168-583X/02/$22.00

Conference Title: Fifteenth International Conference on Ion Beam Analysis (incorporating Twelfth AINSE Conference on Nuclear Techniques of Analysis)
Conference Sponsor: AINSE; Bohmische Phys. Soc.; Elsevier Sci.; High Voltage Eng. Europe; MARCO (Melbourne Univ.); et al
Conference Date: 15-20 July 2001 Conference Location: Cairns, Qld., Australia
Language: English
Abstract: We discuss the excitation and deexcitation processes for solid state optical emitters. At present, there is considerable interest in depositing a material system, which is compatible with Si **microelectronics** processing and which emits electroluminescence (EL). We compare the EL results of rare earth-doped **transistors** in Si with doped insulators and doped wide bandgap semiconductors, especially Er in Si (a **source** for 1.5 mu m) as well as Er and Tb in SiO/sub 2/, Si/sub 3/N/sub 4/ and AlN, which are sources for infrared and visible light. The most impressive results are achieved by RE-doped GaN film devices, which cover the entire visible spectrum.
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44/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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5533246 INSPEC Abstract Number: A9709-7340Q-010, B9705-2530F-021
Title: Low-dose SIMOX approach and stimulating factors
Author(s): Litovchenko, V.; Romanyuk, B.; Efremov, A.; Klyui, M.; Mel'nik, V.P.
Author Affiliation: Inst. of Semicond. Phys., Acad. of Sci., Kiev, Ukraine
Conference Title: Proceedings of the Seventh International Symposium on Silicon-On-Insulator Technology and Devices p.117-20
Editor(s): Hemment, P.L.F.; Cristoloveanu, S.; Izumi, K.; Houston, T.; Wilson, S.
Publisher: Electochem. Soc, Pennington, NJ, USA
Publication Date: 1996 Country of Publication: USA ix+440 pp.
Material Identity Number: XX96-02880
Conference Title: Proceedings of Seventh International Symposium on Silicon-on- Insulator Technology and Devices
Conference Date: 5-10 May 1996 Conference Location: Los Angeles, CA, USA
Language: English
Abstract: The conventional SIMOX method for creation of SOI structures in Si needs either very high doses of implanted oxygen together with very high annealing temperatures, or lower implantation doses using multistage implantation-annealing procedures. Recently, a new set approaches were proposed to improve this technology and achieve a thin **buried oxide** layer. In particular, high-dose Ar/sup +/ preimplantation or combined (O/sup +/+N/sup +/) implantation were used, mostly in order to compensate for mechanical stress induced by the difference between Si-Si and Si-O chemical bonds length. In previous presentations, we have also proposed a combined (O/sup +//sub 2/+C/sup +/) implantation. In this case, the carbon dissolved in the Si matrix plays a triple role: firstly as a compensator for atomic volume misfit and thus for the macroscopic strain and stress induced after SiO/sub 2/ precipitation, secondly as a source of excess vacancies (or vacancy clusters), and finally as a getter which attracts oxygen and in such a manner facilitates the SiO/sub 2/ phase creation.
Subfile: A B
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44/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
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5046783 INSPEC Abstract Number: A9520-6170T-007, B9510-2530C-070
Title: A **SI/n** /sup +/ structure in semi-insulating GaAs substrate by high energy implantation
Author(s): Han Dejun; Chan, K.T.; Li Guohui; Wang Wenxun; Zhu Enjun
Author Affiliation: Dept. of Electron. Eng., Hong Kong Univ., Hong Kong
Journal: Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) vol.B100, no.1 p.65-8
Publication Date: May 1995 Country of Publication: Netherlands
CODEN: NIMBEU ISSN: 0168-583X
U.S. Copyright Clearance Center Code: 0168-583X/95/$09.50
Language: English
Abstract: A structure that consists of a semi-**insulating** layer over a **buried** n/sup +/ layer (**SI/n**/sup +/) has been obtained by MeV Si/sup +/ implantation into SI-GaAs substrate and subsequently tailored by a very low dose O/sup +/ implantation. This novel structure has been studied by measurements of current-voltage characteristics, electrochemical C-V profiling and Hall effects. The results indicate that this structure is suitable for the provision of isolation, the fabrication of active devices and internal interconnections.
Subfile: A B
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44/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC
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4956811 INSPEC Abstract Number: B9507-2570-004
Title: A semi-insulating/n/sup +/-structure in GaAs substrates by high energy implantation
Author(s): Han Dejun; Chan, K.T.; Li Guohui; Wang Wenxun; En-Jun Zhu
Author Affiliation: Dept. of Electron. Eng., Chinese Univ. of Hong Kong, Shatin, Hong Kong
p.58-61
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA vi+65 pp.
ISBN: 0 7803 2086 7
U.S. Copyright Clearance Center Code: 0 7803 2086 7/94/$4.00
Conference Title: 1994 IEEE Hong Kong Electron Devices Meeting
Conference Sponsor: IEEE Electron Devices Soc.; Hong Kong Univ. Sci. & Technol
Conference Date: 18 July 1994 Conference Location: Hong Kong
Language: English
Abstract: A structure that consists of a semi-**insulating** layer over a **buried** n/sup +/ layer (**SI/n**/sup +/) has been obtained by MeV Si/sup +/ implantation into SI-GaAs substrates and subsequently tailored by a very low dose O/sup +/ implantation. This novel structure has been studied by measurements of current-voltage characteristics, electrochemical C-V profiling and Hall effects. The results indicate that this structure is suitable for the provision of isolation, the fabrication of active devices and internal interconnections.
Subfile: B
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44/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC
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4950177 INSPEC Abstract Number: B9506-2530F-022
Title: Properties of silicon-on-insulator structures obtained by laser zone melting of polysilicon
Author(s): Lysenko, V.S.; Nazarov, A.N.; Rudenko, T.E.; Rudenko, A.N.; Kil'chitskaya, V.I.; Givargizov, E.I.; Limanov, A.B.
Author Affiliation: Inst. of Semicond. Electron., Acad. of Sci., Ukraine
Journal: Mikroelektronika vol.23, no.6 p.32-8
Publication Date: Nov.-Dec. 1994 Country of Publication: Russia
CODEN: MKETA9 ISSN: 0544-1269
Translated in: Russian Microelectronics vol.23, no.6 p.333-8
Publication Date: Nov.-Dec. 1994 Country of Publication: USA
CODEN: RUICE5 ISSN: 1063-7397
U.S. Copyright Clearance Center Code: 1063-7397/94/2306-0333$12.50
Language: English
Abstract: High-temperature laser zone melting was used to produce silicon films on various multilayer insulators with **silicon nitride** (Si/sub 3/N/sub 4/) and oxynitride (Si/sub x/O/sub y/N/sub z/) interlayers. **Integrated-circuit** components were fabricated on the basis of the silicon-on-insulator (SOI) structures obtained. The electrophysical properties of the components were studied by means of the current-voltage and voltage-capacitance characteristics; the changes in the chemical composition of the **buried insulators** after laser zone melting were studied by secondary-ion mass spectrometry. The results demonstrated the feasibility of fabricating silicon films and **transistors** with rather good properties on multilayer insulators and showed that multilayer insulators with oxynitride interlayers poorly accumulate positive charge under irradiation.
Subfile: B
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44/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC
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02323309 INSPEC Abstract Number: B84052273
Title: The elimination of devitrification defects in antimony buried-layer diffusions
Author(s): Alvarez, A.R.; Pintchovski, F.
Author Affiliation: Motorola Semiconductor Inc., Mesa, AZ, USA
Journal: Journal of the Electrochemical Society vol.131, no.6 p. 1438-40
Publication Date: June 1984 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
Language: English
Abstract: Doped silicate glasses are widely used as diffusion sources for buried layers in bipolar technology. Thermal oxide is commonly used as a diffusion mask in these processes. More recently, the use of **silicon nitride/silicon dioxide** as a diffusion barrier for this application has been reported. During the diffusion of boron, phosphorus, arsenic, and antimony from doped glass sources, a common type of glass damage occurs, devitrification, and this damage propagates into the silicon substrate. The authors describe a composite Si/sub 3/Ni/sub 4//SiO/sub 2/ diffusion mask. This mask was found to greatly decrease the levels of devitrification damage induced by antimony diffusions from a doped glass **source** . The reduction in defect density at the buried layer led to improved breakdown characteristics in NPN **transistors** and a

concomitant increase in functional circuit yields.
Subfile: B

44/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC
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00768470 INSPEC Abstract Number: B75019908
Title: Fabrication of small contacts to **source** and **drain** of IGFET's
Author(s): De La Moneda, F.H.
Author Affiliation: IBM, New York, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.17, no.8 p.2361-2
Publication Date: Jan. 1975 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: Describes a method employing **silicon nitride** coatings to mask the growth of a thermal **silicon dioxide** layer in the formation of contact via holes.
Subfile: B

44/3,AB/9 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

04453573 Genuine Article#: TD933 Number of References: 27
Title: CHEMICAL FREE ROOM-TEMPERATURE **WAFER** TO **WAFER** DIRECT BONDING (Abstract Available)
Author(s): FARRENS SN; DEKKER JR; SMITH JK; ROBERDS BE
Corporate Source: UNIV CALIF DAVIS,DEPT ELECT ENGN & COMP SCI,ENGN UNIT 2/DAVIS//CA/95616; UNIV CALIF DAVIS,DEPT CHEM ENGN & MAT SCI,ENGN UNIT 2/DAVIS//CA/95616
Journal: JOURNAL OF THE ELECTROCHEMICAL SOCIETY, 1995, V142, N11 (NOV), P 3949-3955
ISSN: 0013-4651
Language: ENGLISH Document Type: ARTICLE
Abstract: A limitation to the use of direct **wafer** bonding methods for micromachining and thin film device manufacturing has been the necessity for high temperature anneals to strengthen the bonded interface. Obviously, strong interface strength is needed to withstand backthinning processes and the rigors of device fabrication. Unfortunately, the elevated temperature exposure has a detrimental effect on implanted or diffused etch stop layers via diffusive broadening. Additionally, for many micromachined applications **wafer** bonding could be used as a final assembly step, replacing epoxies. However, the sensitive components of the device must be protected from thermal effects. This paper describes the use of oxygen plasmas to develop chemical free, room temperature, **wafer** to **wafer** bonding methods. The bond developed between plasma-activated silicon **wafers** is virtually at full strength upon contact bonding and does not require further thermal strengthening. The results for **silicon dioxide** bonding show that full strength material is achieved with anneals below 300 degrees C. This process has been applied to a number of **wafer** materials including sapphire, **silicon dioxide**, **silicon nitride**, and gallium arsenide. The data presented are the results of strength tests, interfacial defect etching, transmission electron microscopy analysis, initial interface reaction kinetics, and mechanisms studies. We also show preliminary results from a suggested

model to explain the observed increases in kinetics compared to conventional aqueous solution processing of samples.

44/3,AB/10 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

00702580 Genuine Article#: EP011 Number of References: 10
Title: RADIATION-INDUCED CHARGE TRAPPING IN IMPLANTED BURIED OXIDES (Abstract Available)
Author(s): BRADY FT; LI SS; KRULL WA
Corporate Source: UNIV FLORIDA,DEPT ELECT ENGN/GAINESVILLE//FL/32611; HARRIS CORP,SEMICOND/MELBOURNE//FL/32901
Journal: JOURNAL OF APPLIED PHYSICS, 1990, V68, N12, P6143-6149
Language: ENGLISH Document Type: ARTICLE
Abstract: We investigate the response of **buried oxide** layers formed by oxygen implantation to total dose x-ray irradiation. The characterization is based on C-V measurements of the **buried oxide** capacitor and on back-channel **transistor** measurements. Reduced charge trapping is found for material implanted with a lower oxygen dose, annealed at higher temperatures, and annealed for longer times. Also, total-dose irradiation was found to generate few interface traps. A particularly interesting result is that an increase in the concentration of shallow donors with x-ray dose was observed for certain samples. This increase in the donor concentration was observed only in the top Si film.

44/3,AB/11 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2002 INIST/CNRS. All rts. reserv.

15722811 PASCAL No.: 02-0432635
From PSI -MOSFET with silicon on oxide to PSI -MOSFET with silicon carbide on nitride
Diamond 2001 : Proceedings of the 12th European Conference on Diamond, Dia mond-like Materials, Carbon Nanotubes, Nitrides & Silicon Carbide
RAVARIU C; RUSU A; RAVARIU F; DOBRESCU D; DOBRESCU L
ROBERTSON John, ed; KAWARADA Hiroshi, ed; KOHN Erhard, ed; SITAR Zlatko, ed
Politehnica' University of Bucharest, 313 Splaiul Independentei, 77206, Bucharest, Romania; National Institute for Research and Development in Microtechnologies (IMT Bucharest), Str.Erou lancu Nicolae 32B, 72996 Bucharest, Romania
Diamond 2001: European conference on Diamond, Diamond-like Materials, Carbon Nanotubes, Nitrides and Silicon Carbide, 12 (Budapest HUN) 2001-09-02
Journal: Diamond and related materials, 2002, 11 (3-6) 1268-1271
Language: English
The PSI -MOSFET is a device used in SOI electrical characterization. The aim of this paper was to establish a comparison between these transistors made in four variants: (1) with silicon film on **buried oxide**; (2) with silicon carbide film on **buried oxide**; (3) with silicon film on buried nitride; and (4) with silicon carbide film on buried nitride. ATLAS software simulated these structures. Besides this virtual experiment, a more complex model for the flat-band voltage is provided.

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12/04/2002

44/3,AB/12 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2002 INIST/CNRS. All rts. reserv.

14233328 PASCAL No.: 99-0435011
Thermally conductive EMC (Epoxy Molding Compound) for **microelectronic** encapsulation
WONHO KIM; BAE J W; CHOI I D; KIM Y S
Dept. of Chemical Engineering, Pusan National University, Pusan 609-735, Korea, Republic of; Dept. of Material Engineering, Korea Maritime University, Pusan, Korea, Republic of; Dept. of Material Engineering, Honglk University, Seoul, Korea, Republic of
Journal: Polymer engineering and science, 1999, 39 (4) 756-766
Language: English
Owing to the trend of faster and denser circuit design, the dielectric properties of packaging materials for semi-conductors will have greater influence on performance and reliability. Also, as **chips** become more densely packaged, thermal dissipation becomes a critical reliability issue. Consequently, four important properties for manufacturing semi-conductor packaging are: low values of dielectric constants, high values of thermal conductivity, relatively low values of thermal expansion coefficients, and low cost. Thus, in this study, AlN (Aluminum Nitride) was selected as the filler for an epoxy matrix to achieve increased performance of an EMC. As a result, the thermal conductivity of an EMC filled with 70 vol% of AlN increased as much as 7-8 times compared with the EMC filled with a crystalline **silica** (vol. 70 %). When more than 60 vol% of AlN was added to the EMC, the dielectric constants and thermal expansion coefficient decreased rapidly.

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44/3,AB/13 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2002 INIST/CNRS. All rts. reserv.

09599086 PASCAL No.: 91-0389529
Buried stacked **insulator** : new soi-structure formed by ion beam synthesis
SKORUPA W; SCHOENEICH J; DE VEIRMAN A; ALBRECHT J
Cent. inst. nuclear res., dep. K.F., Dresden 8051, Federal Republic of Germany
Journal: Electronics letters, 1991, 27 (3) 202-204
Language: English
The formation of a new SOI-structure is proposed and the first experimental results are presented. Using high dose implantation of nitrogen and oxygen, a buried stacked layer consisting of **silicon dioxide** (upper part), silicon oxynitride (medium part) and **silicon nitride** (lower part) was formed in single crystalline silicon

FILE 'REGISTRY'

L1 48 S O2SI/MF

L2 6 S NSI/MF FILE 'HCAPLUS'

L3 580191 S (SILICON OR SI)(W)(DIOXIDE OR O2) OR
SILICA OR MYRICKITE OR TRIDYMITE OR BOBKOVITE OR
MOGANITE OR
QUARTZ OR CRISTOBALITE OR ADELITE OR ACTICEL OR L1

L4 318001 S ACEMATT OR STISHOVITE OR COESITE OR
SIBELITE OR CRYSVARL OR CR!STOBALITE OR SARDONYX OR
QUARTZINE
OR SIKRON OR MILLISIL OR ROCK(W)CRYSTAL OR SIO2

L5 76507 S (SILICON OR SI)(W)(NITRIDE OR N OR
MONONITRIDE) OR SIN OR SILYLIUM

L6 663 S L2

L7 239343 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRC
UIT)) OR (MICRO)(W)(CIRCUIT OR CHIP OR ELECTRONIC?) OR CHIP
OR
MICROCIRCUIT OR DIE OR LOGIC(W) CIRCUIT OR WAFER OR
MICROELECTR
ONIC? OR DICE

L8 82930 S TRANSISTOR

L9 4755 S (BURY### OR BURIED OR ENCAPSUL? OR CAPSUL?
OR ENCAS?)(3A)(OXIDE OR INSULAT? OR DIELECTRIC)

L10 31 S (BRYANT, ANDRES OR BRYANT ANDRES OR
BRYANT, A OR BRYANT A)/AU

L11 3 S (JAFFE, M D OR JAFFE M D OR JAFFE, MARK D
OR JAFFE MARK D.)/AU

L12 43 S (JAFFE, M OR JAFFE M OR JAFFE, MARK OR
JAFFE MARK)/AU

L13 26122 S ((L3 OR L4)) AND ((L5 OR L6))

L14 1326 S L7 AND L8 AND L13

L15 193 S L14 AND (DRAIN)(3A)(STRUCTURE OR REGION OR
AREA OR ZONE)

L16 174 S L15 AND (SOURCE)(3A)(STRUCTURE OR REGION
OR AREA OR ZONE)

L17 9 S L16 AND BODY

L18 3 S L16 AND RECESS

L19 5 S L16 AND (SINGLE OR ONE OR 1 OR ONLY)(3A)(CR
YSTAL)

L20 8 S (L19 OR L18) NOT L17

L21 1 S (L10 OR L11 OR L12) AND L14

L22 2 S (L10 OR L11 OR L12) AND L13

L23 2 S L21 OR L22

L24 5863 S ((L3 OR L4))(15A)((L5 OR L6))

L25 5052 S L13(7A)L8

L26 8900 S L5 AND L7

L27 1711 S L26 AND L8
L28 1325 S L27 AND L13
L29 5 S L16 AND (SINGLE OR ONE OR 1 OR ONLY)(3A)(CR
YSTAL)
L30 35 S L28 AND (SINGLE OR ONE OR 1 OR ONLY)(3A)(CR
YSTAL)
L31 30 S L30 NOT ((L17 OR L18 OR L19 OR L20 OR L21
OR L22 OR L23))
L32 1 S L28 AND (TOP OR UPPER)(3A)BODY
L33 0 S L28 AND (LOWER OR BOTTOM)(3A)BODY
L34 26 S L28 AND BODY
L35 16 S L34 NOT ((L17 OR L18 OR L19 OR L20 OR L21
OR L22 OR L23) OR L31)
L36 185 S L28 AND (SOURCE)(3A)(STRUCTURE OR REGION
OR AREA OR ZONE)
L37 21 S L28 AND (SOURCE)(A)(STRUCTURE OR REGION OR
AREA OR ZONE)
L38 170 S L28 AND (SOURCE)(2A)(STRUCTURE OR REGION
OR AREA OR ZONE)
L39 174 S L36 AND (DRAIN)(3A)(STRUCTURE OR REGION OR
AREA OR ZONE)
L40 161 S L38 AND (DRAIN)(2A)(STRUCTURE OR REGION OR
AREA OR ZONE)
L41 156 S L28 AND (DRAIN)(A)(STRUCTURE OR REGION OR
AREA OR ZONE)
L42 147 S L41 AND (SOURCE)(2A)(STRUCTURE OR REGION
OR AREA OR ZONE)
L43 0 S L42 AND FIN

FILE 'REGISTRY'
L44 5 S SI/CN
L45 1 S SILICON/CN

FILE 'HCAPLUS'
L46 110233 S (HEXSILCN OR METASILICON OR POLYSILICONCN
OR SICOMILL OR SILGRAIN OR SILICON OR SILSO OR L45 OR SI OR
L44)(2A)(LAYER? OR FILM OR COAT)
L47 110233 S (HEXSIL OR METASILICON OR POLYSILICONCN OR
SICOMILL OR SILGRAIN OR SILICON OR SILSO OR L45 OR SI OR
L44)(2A)(LAYER? OR FILM OR COAT)
L48 40 S L42 AND L47
L49 21 S L37 NOT ((L17 OR L18 OR L19 OR L20 OR L21
OR L22 OR L23) OR L31 OR L34)
L50 32 S L48 NOT ((L17 OR L18 OR L19 OR L20 OR L21
OR L22 OR L23) OR L31 OR L34 OR L37)

FILE 'WPIX, JAPIO'

L51 202214 S (SILICON OR SI)(W)(DIOXIDE OR O2) OR
SILICA OR MYRICKITE OR TRIDYMITE OR BOBKOVITE OR
MOGANITE OR
QUARTZ OR CRISTOBALITE OR ADELITE OR ACTICEL

L52 71082 S ACEMATT OR STISHOVITE OR COESITE OR
SIBELITE OR CRYSVARL OR CR!STOBALITE OR SARDONYX OR
QUARTZINE
OR SIKRON OR MILLISIL OR ROCK(W) CRYSTAL OR SIO2

L53 50111 S (SILICON OR SI)(W)(NITRIDE OR N OR
MONONITRIDE) OR SIN OR SILYLIUM OR SIN

L54 883948 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRC
UIT)) OR (MICRO)(W)(CIRCUIT OR CHIP OR ELECTRONIC?) OR CHIP
OR
MICROCIRCUIT OR DIE OR LOGIC(W) CIRCUIT OR WAFER OR
MICROELECTR
ONIC?

L55 313650 S TRANSISTOR

L56 3539 S (BURY### OR BURIED OR ENCAPSUL? OR CAPSUL?
OR ENCAS?)(2N)(OXIDE OR INSULATE OR DIELECTRIC)

L57 126392 S (HEXSIL OR METASILICON OR POLYSILICONCN OR
SICOMILL OR SILGRAIN OR SILICON OR SILSO OR SI OR
L44)(2N)(LAYE
R? OR FILM OR COAT?)

L58 40 S (BRYANT, ANDRES OR BRYANT ANDRES OR
BRYANT, A OR BRYANT A)/AU

L59 11 S (JAFFE, M OR JAFFE M OR JAFFE, MARK OR
JAFFE MARK)/AU

L60 51 S (L58 OR L59)

L61 0 S L60 AND ((L51 OR L52)) AND L53

L62 6606 S (L51 OR L52) AND L53

L63 651 S L54 AND L56

L64 137 S L63 AND L55

L65 137 S L64 AND L56

L66 36 S L65 AND (DRAIN)(2N)(STRUCTURE OR REGION OR
AREA OR ZONE)

L67 39 S L65 AND (SOURCE)(2N)(STRUCTURE OR REGION
OR AREA OR ZONE)

L68 41 S L66 OR L67

L17 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:616101 HCAPLUS
DN 137:162431
TI Open bit line DRAM with ultra thin **body transistors**
IN Forbes, Leonard; Ahn, Kie Y.
PA Micron Technology, Inc., USA
SO U.S. Pat. Appl. Publ., 31 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002109176	A1	20020815	US 2001-780125	20010209

AB Structures and method for an open bit line DRAM device are provided. The open bit line DRAM device includes an array of memory cells. Each memory cell in the array of memory cells includes a pillar extending outwardly from a semiconductor substrate. The pillar includes a single cryst. first contact layer and a single cryst. second contact layer sepd. by an oxide layer. In each memory cell a single cryst. vertical **transistor** is formed along side of the pillar. The single cryst. vertical **transistor** includes an ultra thin single cryst. vertical first **source/drain region** coupled to the first contact layer, an ultra thin single cryst. vertical second **source/drain region** coupled to the second contact layer, an ultra thin single cryst. vertical **body** region which opposes the oxide layer and couples the first and the second **source/drain regions**, and a gate opposing the vertical **body** region and sepd. therefrom by a gate oxide. A plurality of buried bit lines are formed of single cryst. semiconductor material and disposed below the pillars in the array memory cells for interconnecting with the first contact layer of column adjacent pillars in the array of memory cells. Also, a plurality of word lines are included. Each word line is disposed orthogonally to the plurality of buried bit lines in a trench between rows of the pillars for addressing gates of the single cryst. vertical **transistors** that are adjacent to the trench.

L17 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:570680 HCAPLUS
DN 137:118044
TI Switching speed improvement in DMOS power **transistor** in the fabrication of a MOSFET LSI
IN Hshieh, Fwu-Iuan
PA Magepower Semiconductor Corp., USA
SO U.S., 19 pp., Division of U.S. Ser. No. 982,848.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6426260	B1	20020730	US 2000-655165	20000905
PRAI	US 1997-982848	A3	19971202		

AB The preset invention discloses an improved method for fabricating a MOSFET **transistor** on a substrate to improve the device ruggedness. The fabrication method includes the steps of: (a) forming an epitaxial layer of a first cond. type as a **drain region** on the substrate and then growing an gate oxide layer over the layer; (b) depositing an overlaying polysilicon layer thereon and applying a polysilicon mask for etching the polysilicon layer to define a plurality

of polysilicon gates; (c) removing the polysilicon mask and then carrying out a **body** implant of a second cond. type followed by performing a **body** diffusion for forming a plurality of **body** regions; (d) performing a high-energy **body**-cond.-type-dopant implant, eg., boron implant, to form a plurality of shallow low-concn. **regions** of **source**-cond.-type, e.g., n-regions, under each of e gates. A DMOS power device with improved switching speed is provided with reduced gate-to-drain capacitance without causing an increase in either the on-resistance of the threshold voltage.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:522376 HCAPLUS
DN 137:71557
TI Novel method of **body** contact for SOI MOSFET
IN Ang, Ting Cheong; Loong, Sang Yee; Quek, Shyue Fong; Song, Jun
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002089031	A1	20020711	US 2001-755572	20010108

AB A new method for forming a silicon-on-insulator MOSFET while eliminating floating **body** effects is described. A silicon-on-insulator substrate is provided comprising a silicon semiconductor substrate underlying an oxide layer underlying a silicon layer. A first trench is etched partially through the silicon layer and not to the underlying oxide layer. Second trenches are etched fully through the silicon layer to the underlying oxide layer wherein the second trenches sep. active areas of the semiconductor substrate and wherein one of the first trenches lies within each of the active areas. The first and second trenches are filled with an insulating layer. Gate electrodes and assocd. **source** and **drain regions** are formed in and on the silicon layer in each active area. An interlevel dielec. layer is deposited overlying the gate electrodes. First contacts are opened through the interlevel dielec. layer to the underlying **source** and **drain regions**. A second contact opening is made through the interlevel dielec. layer in each of the active regions wherein the second contact opening contacts both the first trench and one of the second trenches. The first and second contact openings are filled with a conducting layer to complete formation of a silicon-on-insulator device in the fabrication of **integrated circuits**.

L17 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:505359 HCAPLUS
DN 137:71446
TI **Transistor structure** having silicide **source**/**drain** extensions in MOSFET **IC**
IN Cheng, Peng; Doyle, Brian; Bai, Gang
PA USA
SO U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

12/04/2002

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PI   US 2002086505     A1   20020704      US 1999-343293   19990630
     US 2002060346     A1   20020523      US 2001-947155   20010905
PRAI US 1999-343293    A3   19990630
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AB The invention relates to a process for making a MOSFET **integrated circuit**, comprising a double silicided **source/ drain structure**, wherein the **source/ drain** terminals include a silicided source/drain extension, a deep silicided **source/drain region**, and a doped semiconductor portion that surrounds a portion of the **source/ drain structure** such that the suicides are isolated from the MOSFET **body** node. In a further aspect of the present invention, a barrier layer is formed around a gate electrode to prevent elec. shorts between a silicided source/drain extension and the gate electrode. A deep source/drain is then formed, self-aligned to sidewall spacers that are formed subsequent to the silicidation of the source/drain extension.

L17 ANSWER 5 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:451031 HCAPLUS
DN 135:39694
TI Method of manufacturing low and high voltage CMOS **transistors** with EPROM cells in the same circuit with fewer steps
IN Palumbo, Elisabetta; Peschiaroli, Daniela; Zatelli, Nicola
PA Stmicroelectronics S.r.l., Italy
SO Eur. Pat. Appl., 10 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

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     PATENT NO.       KIND  DATE          APPLICATION NO.  DATE
     ---------------  ----  --------      ---------------  --------
PI   EP 1109217       A1    20010620      EP 1999-830770   19991213
         R:  AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,
             IE, SI, LT, LV, FI, RO
```

AB The **body** regions for the n-channel and p-channel LV **transistors**, for the n-channel HV **transistors**, and for the EPROM cells are formed on a Si substrate; a thermal oxide layer (12) is formed and a layer of polycryst. Si (13) is formed thereon; the latter layer is selectively removed to form the floating gate electrodes (13a) of the cells and the gate electrodes (13b) of the HV **transistors;** the **source** and **drain regions** (14) of the cells, the **source** and **drain regions** (22) of the n-channel HV **transistors,** the **body regions** (24) and the **source** and **drain regions** of the p-channel HV **transistors** are formed; an ONO composite layer (15) is formed; the Si of the areas of the LV **transistors** is exposed; a thermal oxide layer is formed on the exposed areas; a 2nd polycryst. Si layer (17) is deposited and is then removed selectively to form the gate electrodes of the LV **transistors** (17c) and the control gate electrodes (17a) of the cells, and the **source** and **drain regions** of the LV **transistors** are formed. By virtue of the use of (ONO) which is impermeable to the O atoms of the subsequent thermal oxidn. and because the **body** regions (24) of the p-channel HV **transistors** and the **source** and **drain regions** of all of the HV **transistors** are produced by sep. implantations, components of very good quality are produced with few more masks than a conventional LV method.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 6 OF 9 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:396574 HCAPLUS
DN 134:374957
TI Process for the fabrication of an **integrated circuit** comprising low and high voltage MOS **transistors** and EPROM cells
IN Crivelli, Barbera; Peschiaroli, Daniela; Palumbo, Elisabetta; Zatelli, Nicola
PA STMicroelectronics S.r.l., Italy
SO Eur. Pat. Appl., 8 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1104022	A1	20010530	EP 1999-830742	19991129
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 2001018250	A1	20010830	US 2000-727266	20001129
	US 6319780	B2	20011120		
PRAI	EP 1999-830742	A	19991129		

AB The active areas and the **body** regions for the LV MOS **transistors**, for the HV MOS **transistors** and for the EPROM cells are formed on a silicon substrate. A layer of thermal oxide is formed, and a layer of polycryst. silicon is formed on it. The last-mentioned layer is removed selectively to form the floating gate electrodes of the cells, the **source** and **drain regions** of the cells are formed, and the silicon of the areas of the HV MOS **transistors** is exposed. A layer of HTO oxide is formed and nitrided, and the silicon of the areas of the LV MOS **transistors** is exposed. A layer of thermal oxide is formed on the exposed areas, a second layer of polycryst. silicon is deposited and is then removed selectively to form the gate electrodes of the LV and HV MOS **transistors** and the control gate electrodes of the cells. Finally, the **source** and **drain regions** of the LV and HV MOS **transistors** are formed. Owing to the simultaneous formation of the gate dielec. of the HV MOS **transistors** and the intermediate dielec. of the cells, and the use of a material (nitrided HTO oxide) which is impermeable to the oxygen atoms of the subsequent thermal oxidn., the no. of the operations in the process is smaller than in the prior art process.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 7 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:396573 HCAPLUS
DN 134:374956
TI Process for the fabrication of **integrated circuits** with low voltage MOS **transistors**, EPROM cells and high voltage MOS **transistors**
IN Palumbo, Elisabetta; Peschiaroli, Daniela; Zatelli, Nicola
PA STMicroelectronics S.r.l., Italy
SO Eur. Pat. Appl., 9 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1104021	A1	20010530	EP 1999-830741	19991129
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				

AB The active areas and the **body** regions for the LV MOS **transistors**, for the HV MOS **transistors** and for the EPROM cells are formed on a silicon substrate, and a layer of thermal oxide is formed and a layer of polycryst. silicon is formed on it. The last-mentioned layer is removed selectively to form the floating gate electrodes of the cells, and the **source** and **drain regions** of the cells are formed. A composite ONO layer is formed, the silicon of the areas of the LV MOS **transistors** is exposed, and a layer of thermal oxide is formed on the exposed areas. A second layer of polycryst. silicon is deposited and is then removed selectively to form the gate electrodes of the LV and HV MOS **transistors** and the control gate electrodes of the cells, and the **source** and **drain regions** of the LV and HV MOS **transistors** are formed. Owing to the simultaneous formation of part of the gate dielec. of the HV MOS **transistors** and the intermediate dielec. of the cells, and the use of a material (ONO) which is impermeable to the oxygen atoms of the subsequent thermal oxidn., the no. of the operations in the process is smaller than in the prior art process.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 8 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:301017 HCAPLUS
DN 134:304217
TI Field effect **transistor** with non-floating **body** and method for forming same on a bulk silicon **wafer**
IN Ju, Dong-hyuk
PA Advanced Micro Devices, Inc., USA
SO PCT Int. Appl., 14 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001029897	A1	20010426	WO 2000-US26165	20000921
	W: CN, JP, KR, SG				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 2002025636	A1	20020228	US 1999-421305	19991020
	US 6376286	B1	20020423		
	EP 1173892	A1	20020123	EP 2000-963752	20000921
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
PRAI	US 1999-421305	A	19991020		
	WO 2000-US26165	W	20000921		

AB A Si on insulator (SOI) field effect **transistor** (FET) structure is formed on a conventional bulk Si **wafer**. The structure includes an elec. coupling between the channel region of the FET with the bulk Si substrate to eliminate the floating **body** effect caused by charge accumulation in the channel regions due to historical operation of the FET. The method of forming the structure includes isolating the FET active region from other structures in the Si substrate by forming an insulating trench about the perimeter of the FET and forming an undercut beneath the active region to reduce or eliminate junction capacitance between the **source** and **drain regions** and the Si substrate.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 9 OF 9 HCAPLUS COPYRIGHT 2002 ACS

12/04/2002

AN 1972:29085 HCAPLUS
DN 76:29085
TI Semiconductor devices provided with protective coverings
IN Gregor, Lawrence V.; Hu, Shih-Ming; Marvel, Robert F.; Petrak, John R.
PA International Business Machines Corp.
SO Brit., 8 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 1196149		19700624		
PRAI	US		19661010		

AB Protective coverings are provided for semiconductor devices by employing a composite Si oxide/Si_3N_4 layer. Thus, in an insulated-gate field-effect **transistor**, a thin film of **SiO_2** is formed over a p-type Si **wafer**. A 2nd contiguous coating of Si_3N_4 is deposited over the **SiO_2** film. Apertures are formed conventionally at predetd. locations in a photoresist layer. The remaining portion of the **SiO_2** film may then be removed by conventional etchants to form diffusion windows. The **wafer** is subjected to conventional diffusion to establish **source** and **drain regions** of cond. type opposite that of the **body** and to create p-n junctions. To complete the structure, a thin film of a conductive metal is deposited to form a gate electrode and elec. conductors in a desired pattern over the top surface of the composite film and over the exposed portions of the **source** and **drain regions**. In such metal-insulator-semiconductor structures, the composite film of **SiO_2** and Si_3N_4 provides perfect insulation between the semiconductor substrate and the metallized patterns.

L20 ANSWER 1 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:833448 HCAPLUS
DN 137:331950
TI High voltage MOS **transistor** device and fabrication thereof
IN Lee, Da Soon
PA Hynix Semiconductor Inc., S. Korea
SO U.S. Pat. Appl. Publ., 14 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002160572	A1	20021031	US 2002-132407	20020426
	JP 2002329860	A2	20021115	JP 2001-245277	20010813
PRAI	KR 2001-23182	A	20010428		

AB A high voltage device and a method for fabricating the same are disclosed, which improves voltage-resistant characteristics to protect against high voltage applied to a gate electrode. The high voltage device includes a semiconductor substrate having first, second and third regions, the first region having sidewalls at both sides, and the second and third regions having a height higher than that of the first region at both sides of the first region. A channel region is formed within a surface of the substrate belonging to the first region including some of the sidewalls. A first insulating film is formed on a surface of the first region including the sidewalls. Buffer conductive films are formed to be adjacent to the sidewalls of the first region and isolated from each other. A second insulating film is formed between the buffer conductive films to have a **recess** portion. A third insulating film is formed on an entire surface including the buffer conductive films. A gate electrode, insulated from lower layers by the third insulating film to fill the **recess** portion, is formed to partially overlap the buffer conductive films. Drift regions are resp. formed in the second and third regions to have a first depth, and **source** and **drain regions** are formed in the second and third regions to have a second depth less than the first depth.

L20 ANSWER 2 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:609934 HCAPLUS
DN 137:148827
TI Double SOI device with **recess** etch and epitaxy
IN Assaderaghi, Fariborz; Chen, Tze-Chiang; Muller, K. Paul; Nowak, Edward Joseph; Sadana, Devendra Kumar; Shahidi, Ghavam G.
PA International Business Machines Corporation, USA
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6432754	B1	20020813	US 2001-788979	20010220
	US 2002115240	A1	20020822		

AB The present invention provides various methods for forming a ground-plane SOI device which comprises at least a field effect **transistor** formed on a top Si-contg. surface of a silicon-on-insulator (SOI) **wafer**; and an oxide region present beneath the field effect **transistor**, located in an **area** between **source** and **drain regions** which are formed in said SOI

wafer, said oxide region is butted against shallow extensions formed in said SOI **wafer**, and is laterally adjacent to said **source** and **drain regions**.

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L20 ANSWER 3 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:193834 HCAPLUS
DN 130:203839
TI Damascene method for source drain definition in fabrication of silicon on insulator MOS **transistors**
IN Wanlass, Frank M.
PA USA
SO U.S., 9 pp., Cont.-in-part of U.S. Ser. No. 922,864, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5882958	A	19990316	US 1997-948211	19971009
PRAI	US 1997-922864		19970903		

AB The present invention is a technique for producing Si-on-insulator MOS **transistors** by damascene patterning of **source-drain regions** in a thin film of amorphous Si deposited on a layer of oxide grown on a Si **wafer**, where the oxide was previously etched with a pattern of trenches. The technique provides for the amorphous layer to contact the underlying Si substrate through multiple small oxide openings, where subsequent **transistor** channel regions will align to these openings. After patterning, the **wafer** is annealed in a high temp. cycle, where the regions of amorphous Si in contact with the Si substrate will grow into **single crystal** Si suitable for **transistor** channel regions.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L20 ANSWER 4 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:732026 HCAPLUS
DN 128:29394
TI GaAs recessed-gate field-effect **transistor**
IN Nakajima, Shigeru
PA Sumitomo Electric Industries, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09293735	A2	19971111	JP 1996-102905	19960424

AB The invention relates to a GaAs recessed-gate FET, suited for use in **IC chip**, e.g., MMIC, wherein the source resistance is reduced at a high breakover voltage by forming the **source-drain region** at or above the level of the active layer.

L20 ANSWER 5 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:677242 HCAPLUS
DN 123:72244
TI Selective epitaxial growth of silicon thin films and MOSFETs using thereof
IN Kotaki, Hiroshi; Kakimoto, Seizo; Nakano, Masayuki

PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 19 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07022338	A2	19950124	JP 1993-165385	19930705
	JP 3009979	B2	20000214		

AB In manuf. of semiconductor devices (e.g. MOSFETs), the selective epitaxy of semiconductor thin films (Si) for active regions is carried out by removing the oxide films from the active regions without exposing the **wafer** to air, and forming **single crystal** films carrying the information of the substrate on the active regions on which the oxide films are removed by choosing the conditions that amorphous or polycryst. films growth on other regions using LPCVD method . By removing the amorphous or polycryst. films using selective etching technique, the **source/drain regions** of the **transistor** are formed. As the **single crystal** films are prepd. in the **source/drain regions** of the **transistors** at relatively low temp., the short channel effect of the **transistors** is avoided.

L20 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1980:190190 HCAPLUS
DN 92:190190
TI Semiconductor devices
IN Custode, Frank Z.; Tam, Matthias L.
PA Rockwell International Corp., USA
SO Fr. Demande, 46 pp.
CODEN: FRXXBL
DT Patent
LA French
FAN.CNT 7

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 2428326	A1	19800104	FR 1979-14305	19790605
	GB 2021861	A	19791205	GB 1979-18077	19790524
	GB 2021861	B2	19820929		
PRAI	US 1978-913258		19780606		
	US 1978-909886		19780526		

AB For high-reliability fabrication of large-scale **integrated circuits** on **single-crystal** Si substrates having high densities of FET's [e.g., an area of .apprx.40 (.mu.m)2 per FET in a memory-cell configuration, compared to the usual 130 (.mu.m)2] and polycryst. Si contacts and interconnections characterized by automatic alignment of the contacts for the **source**, gate, and **drain regions**, a new process was developed, which includes formation of **SiO2** (thermally grown), Si3N4, Si oxynitride, and polycryst. Si layers.

L20 ANSWER 7 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1975:507217 HCAPLUS
DN 83:107217
TI Silicon semiconductor device having a field-effect **transistor** with an insulated silicon gate electrode
IN Dingwall, A. G. F.
PA RCA Corp., USA
SO Belg., 18 pp.
CODEN: BEXXAL

DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	BE 818547	A1	19741202	BE 1974-147341	19740806
	IN 140846	A	19761225	IN 1974-CA1265	19740611
	IT 1015392	A	19770510	IT 1974-24412	19740625
	CA 1012658	A1	19770621	CA 1974-204805	19740715
	DE 2436517	A1	19750306	DE 1974-2436517	19740729
	GB 1476790	A	19770616	GB 1974-33315	19740729
	NL 7410214	A	19750210	NL 1974-10214	19740730
	SE 7409993	A	19750207	SE 1974-9993	19740802
	JP 50051276	A2	19750508	JP 1974-89408	19740802
	BR 7406340	A0	19750909	BR 1974-6340	19740802
	FR 2240532	A1	19750307	FR 1974-27142	19740805
	AU 7472061	A1	19760212	AU 1974-72061	19740806
	US 3936859	A	19760203	US 1975-570516	19750422
PRAI	US 1973-385669		19730806		

AB Known techniques were used to fabricate, on a **single-crystal** Si substrate, a flat field-effect **transistor** with an insulated polycryst. Si gate electrode (A) (thickness d = 3000-6000 .ANG.) situated near the top surface of a mesa-shaped region (B) (comprised primarily of the substrate material), and self-aligned with the P-N junctions connecting the **source** and **drain regions** (C) (formed by diffusion doping of the Si substrate) that are situated at the base of region B. The sides of region B are surrounded by a contiguous insulating **SiO2** layer (D) (d .apprxeq. 10,000 .ANG.) thermally grown on top of regions C to facilitate the forming of (and reduce the output losses assocd. with) the interconnecting metallic conductors that cross over and make contact with electrode A. Electrode A is deposited (by pyrolysis of SiH4) on top of a **SiO2** insulating layer (d .apprxeq. 1000 .ANG.) thermally grown on top of region B. On top of A is deposited (by pyrolysis of SiH4 and NH3) an insulating layer of Si3N4 (E) having a thickness such that the top surfaces of layers D and E are at the same level. All of the layers are parallel to the surface of region B. The presence of D allows contact openings to be made through layer E to A, without requiring crit. alignment of the mask or extensive zones of contact. Elec contacts from regions C to other parts of the **integrated circuit** can be formed by etching holes in D and suitably depositing Al films.

L20 ANSWER 8 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1971:92690 HCAPLUS
DN 74:92690
TI Solid state devices and **integrated circuits**
IN Brown, George Axel; Carlson, Harold G.
PA Texas Instruments Inc.
SO S. African, 17 pp.
CODEN: SFXXAB
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	ZA 6908036		19700626		
PRAI	US		19681230		

AB The fabrication of solid state devices and **integrated circuits** is described in detail. The base material is n- or p-type Si doped to a concn. of .apprx.1016 atoms /cm3 sawed from a **single crystal** at .apprx.3-5.degree. from 111

orientation. After customary polishing it is placed in a cold or hot wall reactor and is cleaned by vapor phase etching for .apprx.5 min with 5% HCl in H at m1250.degree.. After purging the reactor with an inert gas such as N or Ar, a **SiO2** layer of 500-1000 .ANG. is formed by heating the substrate in an atm. of d ry O for 2 min at 1100.degree.. After purging the reactor, a layer of **SiN** is formed on this by chem. vapor deposition from a gaseous mixt. of silane and NH3 in H at 850-900.degree.. By carrying out all these operations within the reactor the **SiO2** layer is free of contaminant and the **SiN** layer seals it and protects it from contamination during subsequent processing steps. A 2nd layer of **SiO2** of .apprx.1000-2000 .ANG. is deposited on **SiN** by chem. vapor deposition from a mixt. of silane and O. The exposure or opening of the windows are done either by the use of multiple etching steps or single etchant process. A glaze of a p-type impurity is then formed on the exposed surface for modifying the cond. of the Si substrate in the area when the impurity diffuses into the exposed substrate area to a concn. of .apprx.1019 or 1020 atoms/ cm3. These regions of modified cond. constitute the **source** and the **drain regions**. Concurrently, a surface layer of thermally grown **SiO2** is formed on the exposed areas of the substrate. Thus on an n-type substrate the **source** and **drain regions** are relatively heavily p-doped regions forming a p-channel field effect **transistor** or it can be vice versa when a n-channel field effect **transistor** is obtained.

12/04/2002

L23 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:632756 HCAPLUS
DN 137:178153
TI Method and structure for creating high density buried contact for use with SOI processes for high performance logic
IN **Bryant, Andres**; Lasky, Jerome B.; Nowak, Edward J.; Rankin, Jed H.; Tong, Minh H.
PA International Business Machines Corporation, USA
SO U.S., 18 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6436744	B1	20020820	US 2001-809888	20010316
	JP 2002314094	A2	20021025	JP 2002-52160	20020227
PRAI	US 2001-809888	A	20010316		

AB A semiconductor device is presented having an SOI FET comprising a Si body on an insulating layer on a conductive substrate. A gate dielec. and a gate are provided on a surface of the Si body, and a source and a drain are provided on 2 sides of the gate. A buried body contact to the substrate conductor is provided below a 3rd side of the gate. The buried body contact does not extend to the top surface of the Si body. The body contact is sepd. from the gate by a 2nd dielec. having a thickness typically greater than that of the gate dielec. The body contact is a plug of conductive material, and the 2nd dielec. coats the body contact under the gate. The FET can be used in an SRAM circuit or other type of circuit having a Si-on-insulator (SOI) construction.
RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:39579 HCAPLUS
DN 136:94600
TI Disposable spacer for symmetric and asymmetric Schottky contact to SOI MOSFET
IN **Bryant, Andres**; Lasky, Jerome B.; Leobandung, Effendi; Schepis, Dominic J.
PA International Business Machines Corporation, USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6339005	B1	20020115	US 1999-425394	19991022
	US 2002048841	A1	20020425	US 2001-978528	20011017
PRAI	US 1999-425394	A3	19991022		

AB A Si on insulator transistor is disclosed which has a Schottky contact to the body. The Schottky contact may be formed on the source and/or drain side of the gate conductor. A spacer, with at least a part thereof being disposable, is formed on the sidewalls of the gate conductor. Extension regions are provided in the substrate which extend under the spacer and the gate conductor. Source and drain diffusion regions are implanted into the substrate adjacent to the extension regions. The disposable part of the spacer is then removed to expose a portion of the extension region. A metal layer is formed at least in the extension regions, resulting in the Schottky contact.

12/04/2002

RE.CNT 28 THERE ARE 28 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

12/04/2002

L31 ANSWER 1 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:808398 HCAPLUS
DN 137:318993
TI Method of forming bipolar **transistor** salicided emitter using selective laser annealing
IN Naem, Abdalla
PA National Semiconductor Corporation, USA
SO U.S., 4 pp., Cont.-in-part of U.S. Ser. No. 708,261.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6468871	B1	20021022	US 2001-816824	20010323
	US 6406966	B1	20020618	US 2000-708261	20001107
PRAI	US 2000-708261	A2	20001107		

AB A method is provided for forming a uniformly salicided **single crystal** Si emitter structure without voids and with complete dopant activation using laser annealing in a semiconductor **integrated circuit** bipolar **transistor** structure. The bipolar **transistor** structure includes a collector region that has a 1st cond. type formed in a semiconductor substrate and a base region having a 2nd cond. type, opposite the 1st cond. type, formed in the collector region. A layer of dielec. material is formed on the surface of the base region. An emitter window is opened in the layer of dielec. material to expose a surface area of the base region. A layer of polysilicon is then formed over the layer of dielec. material and extending into the emitter window such that at least a portion of the layer of polysilicon is in contact with the surface area of the base region. Dopant of the 1st cond. type is then introduced into the layer of polysilicon. A region of anti-reflective coating (ARC) material is formed on the layer of polysilicon over the emitter window opening such that portions of the layer of polysilicon are exposed. Sufficient laser energy is then applied to the structure resulting from the foregoing steps to cause the polysilicon underlying the region of anti-reflective coating material to flow and recrystallize. The region of anti-reflective coating material is then used as a hard mask to remove unwanted regions of polysilicon, thereby defining a **single crystal** Si emitter region under the ARC material and extending into the emitter window opening and in interfacial contact with the surface area of the base region. The ARC material is then removed and a layer of refractory metal silicide is formed on the recrystd. polysilicon emitter region.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 2 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:538192 HCAPLUS
DN 137:71582
TI Method for making a monocrystalline substrate and **integrated circuit** comprising such a substrate
IN Menut, Olivier; Gris, Yvon
PA STMicroelectronics S.A., Fr.
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA French
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

12/04/2002

PI EP 1223614 A1 20020717 EP 2002-290038 20020109
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR
FR 2819631 A1 20020719 FR 2001-414 20010112
JP 2002270509 A2 20020920 JP 2001-394184 20011226
PRAI FR 2001-414 A 20010112

AB One manufs. an initial **single-crystal** substrate presenting locally and in a surface at least a discontinuity of the crystal lattice. One hollows the initial substrate horizontal to the discontinuity. **One** amorphizes the **crystal** lattice at the periphery. One deposits on the structure obtained a layer of amorphous material having the same chem. compn. as the initial substrate. One effects thermal annealing of the obtained structure in order to recrystallize the amorphous material in continuity with the **single -crystal** lattice of the initial substrate.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 3 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:771264 HCAPLUS
DN 136:109672
TI Hybrid integration of light-emitters and detectors with SOI-based micro-opto-electro-mechanical systems (MOEMS)
AU Kubby, Joel; Calamita, Jim; Chang, Jen-Tsorng; Chen, Jingkuang; Gulvin, Peter; Lin, C.-C.; Lofthus, Robert; Nowak, Bill; Su, Yi; Tran, Alex; Burns, David; Bryzek, Janusz; Gilbert, John; Hsu, Charles; Korsmeyer, Tom; Morris, Art; Plowman, Ted; Rabinovich, Vladimir; Daiber, Troy; Scharf, Bruce; Zosel, Andrew; Fan, Li; Hartman, Jim; Husain, Anis; Golubovic-Liakopoulos, Nena; Mali, Raji; Pumo, Tom; Delvecchio, Steve; Zhou, Shifang; Rosa, Michel; Sun, Decai
CS Xerox Wilson Reserach Center, Webster, NY, 14580, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (2001), 4293(Silicon-Based and Hybrid Optoelectronics III), 32-45
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English

AB A multidisciplinary team of end users and suppliers has collaborated to develop a novel yet broadly enabling process for the design, fabrication and assembly of Micro-Opto- Electro-Mech. Systems (MOEMS). A key goal is to overcome the shortcomings of the polysilicon layer used for fabricating optical components in a conventional surface micromachining process. These shortcomings include the controllability and uniformity of material stress that is a major cause of curvature and deformation in released microstructures. The approach taken by the consortium to overcome this issue is to use the **single-crystal**-Si (SCS) device layer of a Si-on-insulator (SOI) **wafer** for the primary structural layer. Since optical flatness and mech. reliability are of utmost importance in the realization of such devices, the use of the Si device layer is seen as an excellent choice for devices which rely on the optical integrity of the materials used in their construction. A 3-layer polysilicon process consisting of 2 structural layers is integrated on top of the Si device layer. This add-on process allows for the formation of sliders, hinges, torsional springs, comb drives and other actuating mechanisms for positioning and movement of the optical components. Flip-**chip** bonding techniques are also being developed for the hybrid integration of edge and surface emitting lasers on the front and back surfaces of the Si **wafer**, adding to the functionality and broadly enabling nature of this process. In addn. to process development, the MOEMS manufg. Consortium is extending Micro-Electro-Mech. Systems (MEMS) modeling and simulation design tools into the optical domain, and

using the newly developed infrastructure for fabrication of prototype micro-optical systems in the areas of industrial automation, optical switching for telecommunications and laser printing.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 4 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:673727 HCAPLUS
DN 135:219724
TI Fabrication of semiconductor **integrated circuit**
IN Toyokawa, Shigeya; Yoshida, Seiji; Matsuoka, Masamichi; Hashimoto, Takashi; Kuroda, Kenichi
PA Hitachi Ltd., Japan; Hitachi Super L.S.I. Systems Co., Ltd.
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001250860	A2	20010914	JP 2000-58357	20000303

AB The title method involves thermally oxidizing a **single-crystal** Si substrate to form a first Si oxide film on the substrate, forming a multilayer film of a **Si nitride** film and a second Si oxide film on the first Si oxide film, selectively removing the multilayer film and the first Si oxide film to expose the isolation regions of the substrate while leaving the multilayer film and the first Si oxide film on the element-forming regions of the substrate, trench etching the substrate using the multilayer film as a mask, forming a third Si oxide film on the overall surfaces, polishing the third Si oxide film until the nitride film is exposed, etching the nitride film, etching the third and first Si oxide films, and forming MISFETs in the element-forming regions. The polishing margin is improved by the multilayer film.

L31 ANSWER 5 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:593311 HCAPLUS
DN 135:161059
TI Memory device having a storage region constructed with a plurality of dispersed particulates
IN Nomoto, Kazumasa; Gosain, Dharam Pal; Usui, Setsuo; Noguchi, Takashi
PA Sony Corporation, Japan
SO U.S., 24 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6274903	B1	20010814	US 1999-404479	19990924
	US 2001044185	A1	20011122	US 2001-888862	20010625
	US 6461917	B2	20021008		
PRAI	JP 1998-274983	A	19980929		
	US 1999-404479	A3	19990924		

AB A memory device, a manufg. method thereof, and an **integrated circuit** thereof are provided for storing information over a long period of time even if the memory device is manufd. at low temps. On a substrate made of glass, etc., a memory **transistor** and a selection **transistor** are formed, with a **Si nitride** film and a **SiO2** film in between. The memory **transistor** and the selection **transistor** are connected in

series at a 2nd impurity region. The conduction region for memory of the memory **transistor** is made of non-**single crystal** Si and a storage region comprises a plurality of dispersed particulates made of non-**single crystal** Si. Therefore, elec. charges can be stored partially if a tunnel insulating film has any defects. The tunnel insulating film is formed by exposing the surface of the conduction region for memory to the ionized gas contg. O atoms.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 6 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:606738 HCAPLUS
DN 133:186516
TI Templates for seeding growth of **single crystal** on arrayed nucleation sites defined on nucleation unfriendly substrates
IN Saxena, Arjun N.
PA USA
SO U.S., 31 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6110278	A	20000829	US 1998-131764	19980810
	US 6392253	B1	20020521	US 1999-370100	19990806
PRAI	US 1998-95990P	P	19980810		
	US 1998-131764	A	19980810		

AB A template for seeding growth of a desired **single-crystal** material (e.g., Si, GaAs) is created by passing through a monocryst. channelizing mask, in a channelizing direction thereof, at least one of a nucleation-friendly species (e.g., Si, Ga) and a knock-off species (e.g., Ar, F) for resp. implant of a nucleation-friendly species within or removal of a nucleation-unfriendly material (e.g., **SiO2**) of a supplied substrate. The desired **single-crystal** material is then grown in epitaxial-like manner from the thus-formed seeding-template. In one embodiment, Si ions are projected through a monocryst. Si mask of a selected crystal orientation ((100), or (111)) in its channelizing direction so as to implant the Si ions in a **SiO2** layer of a supplied substrate according to the selected crystal orientation of the channelizing mask. Monocryst. Si is then epitaxially grown on top of the **SiO2** layer with the same crystal orientation. Three-dimensional **integrated circuits** (3-dimensional ULSIC's or UPIC's) may then be formed with this technique. The technique may be extended to many other fields of application that can benefit from economic formation of **single-crystal** materials, such as optics, optoelectronics, tribol., metallurgy, and so forth.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 7 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:565554 HCAPLUS
DN 131:207801
TI Fabrication of a semiconductor device
IN Nakashima, Kazuaki
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11243197	A2	19990907	JP 1998-42058	19980224

AB The invention relates to a process for making a semiconductor device, i.e., a MOS **transistor** LSI, wherein the selective formation of Si film on a **single crystal** Si substrate is achieved by the use of differential etching or oxidn. rate of doped Si.

L31 ANSWER 8 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:409607 HCAPLUS
DN 131:52864
TI Integratable vertical bipolar **transistor**
IN Ehwald, Karl-Ernst; Einbrodt, Wolfgang; Fuernhammel, Felix; Goettlich, Wolfgang
PA Thesys Gesellschaft fuer Mikroelektronik m.b.H., Germany
SO Ger. Offen., 10 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19758339	A1	19990624	DE 1997-19758339	19971222

AB A vertically constructed bipolar **transistor** is described as component of an **integrated circuit**, which can be fabricated by MOS (SOI)- technol. by the application of a **single crystal** semiconductor film on an insulating underlayer. This component has advantages such as frequency response at sufficiently high voltages, at least on the same level as those in logical circuits for elec. switches(early voltages), as well as switching capability and accuracy. The essential fabrication steps are isotope lateral etching of the insulator layer underneath the **single crystal** semiconductor layer(collector area)and the subsequent filling of the subcollector area with CVD deposition of a highly conductive polycryst. material.

L31 ANSWER 9 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:21653 HCAPLUS
DN 130:74859
TI Fabricating a power **transistor** using a silicon-on-insulator (SOI) **wafer**
IN Kang, Wong-gu; Lyu, Jong-son; Kang, Sung-weon
PA Electronics and Telecommunications Research Institute, S. Korea
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5854113	A	19981229	US 1996-742157	19961101

AB Fabricating a power **transistor** using an SOI **wafer** includes forming an SOI layer having a 1st oxide film and a **single -crystal** Si film by implanting O ions in a **single-crystal** substrate and heat-treating, forming source and drain electrodes of a 1st polysilicon film surrounded by a 3rd oxide film on the SOI substrate, forming a shallow junction by ion-implanting the source and drain electrodes, forming a 2nd polysilicon film by reactive ion etching of the 3rd oxide film to form a gate electrode, implanting a p-type dopant

ion using a photoresist film as a mask to supply a voltage to the lower portion of the SOI layer beneath the channel portion, and forming source and drain electrodes.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 10 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:326386 HCAPLUS
DN 127:27474
TI Manufacture of semiconductor apparatus by LOCOS (local oxidation of silicon) method
IN Fujikake, Hideki
PA Nippon Steel Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09082700	A2	19970328	JP 1995-264810	19950919

AB In the manuf., a nitride film is selectively formed on a SIMOX (sepn. by implanted O) **wafer** comprising a laminate of (1st Si **single crystal**/buried oxide film/2nd Si **single crystal**), then the 2nd Si **single crystal** is thermally and selectively oxidized using the nitride film as a mask to form a field oxide film. The method prevents generation of (A) a pinhole in a buffer layer in forming a field oxide film, and (B) micro trench in the Si substrate surface at a region where a MOS **transistor** may be formed.

L31 ANSWER 11 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:434746 HCAPLUS
DN 125:73838
TI Manufacture of MOS-type semiconductor devices
IN Hazama, Hiroaki; Yamabe, Kikuo; Tomita, Hiroshi
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08107192	A2	19960423	JP 1994-241743	19941006

AB The process includes: (1) forming a 1st insulator film on the whole surface of a 1st **single-crystal wafer**, (2) forming a 2nd insulator film on the whole surface of a 2nd **single -crystal wafer**, (3) sticking the 2 **wafers** together, and (4) thinning the 1st **single-crystal wafer**. A **single-crystal** gate electrode for a MOS (metal oxide semiconductor) device is formed, utilizing the 1st **single-crystal wafer** thinned in the step 4. The 1st and 2nd insulator films may be an oxide film formed by oxidizing the **wafers** or an oxynitride film.

L31 ANSWER 12 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:231571 HCAPLUS
DN 124:304335
TI Semiconductor device with SOI substrate and its manufacture
IN Sakakibara, Jun; Mochizuki, Yasuhiro; Asai, Shoki; Tsuruta, Kazuhiro

12/04/2002

PA Nippon Denso Co, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08018054	A2	19960119	JP 1994-117824	19940531
PRAI	JP 1994-91199		19940428		

AB The manuf. involves forming a doped region of shallow junction by diffusion from a raised source drain on a semiconductor substrate. The manuf. involves the following steps: (1) forming a trench with reverse taper shape in a semiconductor substrate, (2) filling the trench with a dielec. to form element isolation region, (3) bonding another semiconductor substrate on the region, (4) polishing the substrate from the backside to form an island-like **single crystal** semiconductor layer, (5) oxidizing the semiconductor layer surface and removing the oxide to remove a damaged layer generated at the polishing, and (6) forming an insulating gate FET. The polishing layer may be coated with a protective layer. The protective layer may be polycryst. Si, **SiO2**, or **Si nitride**. The device shows surface width of the **single crystal** semiconductor layer (W) and that of the element isolation region (W'), W.ltoreq.W'.

L31 ANSWER 13 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:991044 HCAPLUS
DN 124:43444
TI Forming self-aligned field-effect and bipolar **transistors**
IN Tsai, Nun Sian
PA Taiwan Semiconductor Manufacturing Company Ltd., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5466615	A	19951114	US 1993-108225	19930819
	US 5831307	A	19981103	US 1997-802178	19970215
PRAI	US 1993-108225		19930819		
	US 1995-518703		19950824		

AB Three insulator layers are formed over the surface of a **single-crystal** semiconductor substrate and are patterned to form a protective block over the location of the 1st element of the **transistor**. A doped conductive layer is formed on the substrate and on the protective block. A 4th insulator layer is formed on the doped conductive layer. Those portions of the doped conductive layer and the 4th insulator layer that are above the horizontal plane of the top of the 3rd insulator layer are removed. The 3rd insulator layer is removed from the protective block. The structure is heated to form the 2nd and 3rd elements by out-diffusion. Oxide spacers are formed adjacent to the protective block. The protective block is removed. A gate oxide is formed for a field-effect **transistor**. A 2nd conductive layer is formed and patterned on and above the 5th insulator layer, and the elements of the **transistors** are completed with elec. contacts to the elements of the **transistors**.

L31 ANSWER 14 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:698875 HCAPLUS
DN 123:100149

12/04/2002

TI Microelectronic devices using crystalline silicon on glass and their fabrication
IN McCarthy, Anthony M.
PA Regents of the University of California, USA
SO PCT Int. Appl., 21 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9511522	A1	19950427	WO 1994-US11641	19941014
	W: CA, JP				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 5414276	A	19950509	US 1993-137402	19931018
	US 5663078	A	19970902	US 1995-373716	19950117
PRAI	US 1993-137402		19931018		

AB A method for fabricating **microelectronic** devices using **single-crystal** Si overcomes the potential damage that may be caused to the device during high-voltage bonding and employs a metal layer which may be incorporated as part of the **transistor**. This is accomplished such that when the bonding of the Si **wafer** or substrate to the glass substrate is performed, the voltage and current pass through areas where **transistors** will not be fabricated. After removal of the Si substrate, further metal may be deposited to form elec. contacts or add functionality to the devices. By this method, both single and gate-all-around devices may be formed.

L31 ANSWER 15 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:316288 HCAPLUS
DN 123:45720
TI Fabricating an **integrated circuit** with raised diffusions and isolation
IN Hsu, Louis L.; Ogura, Seiki; Shepard, Joseph F.
PA International Business Machines Corp., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5376578	A	19941227	US 1993-169874	19931217
	JP 07202013	A2	19950804	JP 1994-296232	19941130
	JP 2745498	B2	19980428		
PRAI	US 1993-169874		19931217		

AB A method of forming a MOSFET in which the source, drain, and isolation are all raised above the surface of the **single-crystal** Si includes the steps of depositing a blanket gate stack including the gate oxide and a set of gate layers, and then depositing isolation members in apertures etched in the gate stack using the gate oxide as an etch stop. The sidewalls that are used to form an LDD source and drain sep. the gate contact from the source and drain contacts.

L31 ANSWER 16 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1989:164531 HCAPLUS
DN 110:164531
TI Manufacture of complementary metal oxide-semiconductor-type **integrated circuit**
IN Ozaki, Masaharu; Yonehara, Takao
PA Canon K. K., Japan

SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 63265463	A2	19881101	JP 1986-246811	19861017
	JP 2516604	B2	19960724		
	EP 264283	A2	19880420	EP 1987-309125	19871015
	EP 264283	A3	19880928		
	EP 264283	B1	19970910		
	R: DE, FR, GB, IT, NL				
	US 5028976	A	19910702	US 1990-529706	19900529
PRAI	JP 1986-246811	A	19861017		
	US 1987-107469	B1	19871013		
	US 1989-449396	B1	19891207		

AB In the manuf. of the title **integrated circuit** having a 1st-cond.-type MOS **transistor** on a semiconductor substrate, and a 2nd-cond.-type MOS **transistor** on the 1st through a sepn. layer (e.g., Si oxide), a heterogeneous material (e.g., Si3N4 or polycryst. Si) is placed on the layer, where the nucleus-forming d. of the material is sufficiently greater than that of the layer material, and is also sufficiently small such that a single nucleus of a semiconductor material (e.g., Si) can grow in it, a **single-crystal** layer of the semiconductor material is formed from the nucleus, and the 2nd MOS **transistor** is formed in the semiconductor layer. The process can enhance the integration level of the circuit.

L31 ANSWER 17 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:430939 HCAPLUS
DN 109:30939
TI A method for fabricating a compound semiconductor device and a semiconductor circuit
PA Massachusetts Institute of Technology, USA
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 63018661	A2	19880126	JP 1987-146842	19870612
	US 4774205	A	19880927	US 1986-874295	19860613
	EP 250171	B1	19921111	EP 1987-305209	19870612
	R: AT, BE, CH, DE, FR, GB, IT, LI, NL, SE				
	AT 82431	E	19921115	AT 1987-305209	19870612
PRAI	US 1986-874295		19860613		
	EP 1987-305209		19870612		

AB A method for fabricating Group IIIA-VA or IIB-VIA semiconductor and Si elements on a common substrate involves the following: (1) forming the Si element on a selected area of the substrate; (2) forming a protective layer on the Si element and the remaining substrate; (3) opening a hole in the protective layer to expose the surface region of the substrate; (4) forming a compd. semiconductor layer of a **single crystal** on the exposed substrate surface and polycrystals on the protective layer; (5) removing the polycrystals; (6) forming a compd.-semiconductor element on the compd.-semiconductor **single crystal**; and (7) forming ohmic contacts on the elements. The protective layer may be **SiO2** or **SiO2** and Si3N4, and the compd. semiconductor may be GaAs. The compd.-semiconductor element may be an optoelectronic

element such as a LED, laser, or optical detector, or a bipolar or field-effect **transistor**. A method is also described for fabricating Group IIIA-VA or IIB-VIA semiconductor and Si elements having a low-resistance connection region. Semiconductor circuits fabricated by the above methods are also described.

L31 ANSWER 18 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:430708 HCAPLUS
DN 109:30708
TI The cw argon-laser-induced zone-melting recrystallization of thin silicon on oxide
AU Xu, Qiuxia; Ryssel, H.; Goetzlich, J.; Steinberger, H.
CS Inst. Semicond., Acad. Sin., Beijing, Peop. Rep. China
SO Journal of Crystal Growth (1988), 88(3), 383-90
CODEN: JCRGAE; ISSN: 0022-0248
DT Journal
LA English
AB Si on insulator (SOI) technologies offer significant possibilities for high-speed and high-d. **integrated circuit** applications. **Single-crystal** Si islands of 50 .mu.m width and 165 .mu.m length was successfully obtained by a combination of seeding structures, a specially-shaped laser beam spot and locally altered capping layers. No grain boundaries and no sub-grain boundaries were obsd. in the island etched with Secco etchant. The recrystd. film had the same .ltbbrac.100.rtbbrac. crystal orientation as the Si substrate. The layers were smooth on the surface. The Si recrystn. obtained with a CW argon laser is described, and 2 types of seeding structures are compared. The mechanisms of the **single-crystal** seeding growth of these structures are discussed. P-Channel depletion MOSFET's with L = 10 .mu.m and w = 40 .mu.m were fabricated in the recrystd. film. The ID-VD characteristics of the devices were excellent. The surface hole mobility was calcd. to be 170 cm2/V.cntdot.s, the same as for devices fabricated in bulk **single crystal**.

L31 ANSWER 19 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:85758 HCAPLUS
DN 108:85758
TI Method for forming crystals and crystalline articles obtained by this method
IN Matsuyama, Jinsho; Hirai, Yutaka; Ueki, Masao; Sakai, Akira
PA Canon K. K., Japan
SO Eur. Pat. Appl., 29 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 240309	A2	19871007	EP 1987-302788	19870331
	EP 240309	A3	19881005		
	EP 240309	B1	19960828		
	R: AT, BE, CH, DE, ES, FR, GB, GR, IT, LI, LU, NL, SE				
	JP 63044717	A2	19880225	JP 1987-67335	19870320
	CA 1320102	A1	19930713	CA 1987-532959	19870325
	CA 1330191	A1	19940614	CA 1987-533332	19870330
	AU 8770787	A1	19871008	AU 1987-70787	19870331
	AT 142048	E	19960915	AT 1987-302788	19870331
	AU 9170263	A1	19910418	AU 1991-70263	19910204
	AU 651805	B2	19940804		
	US 5593497	A	19970114	US 1995-415580	19950403
	US 5846320	A	19981208	US 1995-468519	19950606

US 5854365	A	19981229	US 1995-575142	19951219

PRAI JP 1986-73093 19860331
JP 1987-67335 19870320
JP 1987-67334 19870320
US 1987-29893 19870325
US 1987-31046 19870327
US 1988-158112 19880216
US 1988-289504 19881223
US 1990-620395 19901130
US 1990-629006 19901218
US 1992-911791 19920710
JP 1993-023469 19930120
JP 1993-095004 19930331
US 1993-139060 19931021
US 1994-182387 19940118

AB A crystal is formed on a substrate having a free surface comprising a nonnucleation surface with small nucleation d. and a nucleation surface exposed, e.g., through the nonnucleation surface, having a higher nucleation d. than the nonnucleation surface and sufficiently small area for **crystal** growth from a **single** nucleus; a **single crystal** is grown from the single nucleus. A no. of nucleation surfaces may be present for growth of a no. of **single crystals** simultaneously or for growth of large-grain polycrystals by allowing the **single crystals** to contact each other. A Si3N4 layer was formed on a Si **single-crystal wafer** and covered with a **SiO2** layer as a nonnucleation surface. The **SiO2** was patterned to expose minute regions of the Si3N4 as nucleation surfaces. Si **single crystals** were grown from SiH2Cl2 at 150 torr and 1030.degree.. All of the **crystals** had **single-crystal** properties of extremely good quality.

L31 ANSWER 20 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:71258 HCAPLUS
DN 102:71258
TI Three-dimensional semiconductor devices utilizing cerium dioxide and ion-implantation
IN Mizutani, Yoshihisa; Takasu, Shinichiro
PA Toshiba Corp., Japan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4479297	A	19841030	US 1982-386808	19820609
PRAI	JP 1981-95344		19810622		

AB A method for fabricating a 3-dimensional multilayer **integrated circuit** of single cryst. CeO2 and Si is proposed. A single-cryst. CeO2 insulation layer, or the like, is formed on a single-cryst. Si substrate. An isolation region is formed in the single-cryst. Si substrate. The region is transformed into a **SiO2** insulation layer by selectively introducing O ions (or N or C ions) through the single cryst. CeO2 insulation layer and reacting the O ions with the single-cryst. Si. An epitaxial Si layer is formed on the **single -crystal** CeO2 insulation layer. Predetd. processes, such as forming a single cryst. CeO2 layer, are performed thereafter to form 3-dimensional structures of semiconductor elements such a MOS **transistors** and bipolar **transistors** with high packing d. and reliability. The elec. potential of driving elements and wiring

formed on the field insulation layer is prevented from influencing the characteristics of the elements around the field insulation layer. The **single-crystal** oxide layer which serves as the gate oxide film of a MOS **transistor** and the field insulation layer is formed on the semiconductor layer at the same time. The field insulation layer may be formed sufficiently thick for a particular device.

L31 ANSWER 21 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1984:620963 HCAPLUS
DN 101:220963
TI Semiconductor device substrate
PA NEC Corp., Japan
SO Jpn. Tokkyo Koho, 5 pp.
CODEN: JAXXAD
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 59033980	B4	19840820	JP 1976-31019	19760322

AB The high-speed compensating insulating gate type **integrated circuit** (CMOS-**IC**) is prepd. by etching polysilicon by HF and forming grooves for **SiO2** barriers, depositing **single -crystal Si N** and P type regions, and forming P-channel field-effect **transistors**. The **SiO2** film is etched to 0.5-1 .mu.m deep.

L31 ANSWER 22 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1982:153962 HCAPLUS
DN 96:153962
TI Junction type field effect semiconductor device and a method of fabricating the same
IN Shinbo, Masafumi
PA Daini Seikoska Co., Ltd., Japan
SO Brit. UK Pat. Appl., 18 pp.
CODEN: BAXXDU
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 2072947	A	19811007	GB 1981-9383	19810325
	GB 2072947	B2	19840905		
PRAI	JP 1980-39460		19800327		
	JP 1980-39464		19800327		

AB An improved method of manufg. high-performance vertical-type static induction **transistors**, FETs, and **integrated circuits** incorporating junction-type field effect devices is described. A drain electrode region of 1 cond. type is formed on the surface of a low impurity-d. **single crystal** region of the same cond. type. A gate region of opposite cond. type encloses the drain region. A polycrystal region is formed on the drain region and a contact window, part of which is detd. by a side oxidn. film, is formed. This contact window is used to receive conducting material connected to the gate region. A multiinsulation island layer of Si3N4 and **SiO2** films is used in the etching of the regions of the device.

L31 ANSWER 23 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1980:190191 HCAPLUS
DN 92:190191
TI **Integrated-circuit** and semiconductor-device

fabrication by ion implantation
IN Godejahn, Gordon C., Jr.
PA Rockwell International Corp., USA
SO Fr. Demande, 30 pp.
CODEN: FRXXBL
DT Patent
LA French
FAN.CNT 7

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 2428325	A1	19800104	FR 1979-14303	19790605
	FR 2428325	B1	19831230		
	US 4221045	A	19800909	US 1978-913184	19780606
	GB 2021863	A	19791205	GB 1979-18080	19790524
	GB 2021863	B2	19830202		
	DE 2922014	A1	19791213	DE 1979-2922014	19790530
	JP 59040296	B4	19840929	JP 1979-67409	19790530
PRAI	US 1978-913184		19780606		
	US 1978-909886		19780526		

AB For high-reliability fabrication of large-scale **integrated circuits** on **single-crystal** Si substrates having high densities of automatically aligned FET's and polycryst. Si contacts and interconnections, a new process is described, which includes formation of **SiO2** (thermally grown), Si3N4, Si oxynitride, and polycryst. Si layers. The process provides for (a) simultaneous doping of several regions (e.g., sources and drains) via ion implantation, (b) formation of a gate floating-contact configuration, (c) diffused conduction lines for interconnecting sources, drains, and isolated contacts of the gates, and (d) direct contacts for sources and drains.

L31 ANSWER 24 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1980:190189 HCAPLUS
DN 92:190189
TI Semiconductor devices
IN Godejahn, Gordon C., Jr.; Heimbigner, Gary L.; Khan, Mahboob K.; Aghishian, Noubar A.
PA Rockwell International Corp., USA
SO Fr. Demande, 37 pp.
CODEN: FRXXBL
DT Patent
LA French
FAN.CNT 7

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 2428358	A1	19800104	FR 1979-14304	19790605
	FR 2428358	B1	19831209		
	US 4192059	A	19800311	US 1978-913257	19780606
PRAI	US 1978-913257		19780606		

AB For high-reliability fabrication of large-scale **integrated circuits** on **single-crystal** Si substrates having automatically aligned polycryst. Si contacts and interconnections and an increased FET d. (e.g., a direct-access-memory **chip** with a capacity of 256 kilobits, compared to the usual 32 kilobits), a new process was developed, which includes (a) thermal growth of a **SiO2** layer, (b) formation of a Si3N4 layer, (c) formation of a Si oxynitride layer, and (d) formation of a polycryst. Si layer. In the process, protective buttons of Si3N4 + Si oxynitride play an important role in automatic alignment of the FET's, the gate electrodes of which contain **SiO2** and polycryst. Si layers.

L31 ANSWER 25 OF 30 HCAPLUS COPYRIGHT 2002 ACS

AN 1970:503525 HCAPLUS
DN 73:103525
TI Preparation of semiconductor devices consisting of a surface at least partially covered by an oxide layer
IN Kooi, Else
PA N. V. Philips' Gloeilampenfabrieken
SO Ger. Offen., 69 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 1809817		19691211		
PRAI	NL		19671121		

AB Two methods are described for the prepn. of **SiO2** layers on semiconducting Si devices, whereby the **SiO2** surface is partially covered by a Si3N4 layer. In the 1st method, a Si **single crystal** was oxidized with dry O at 1200.degree. and cooled in N, yielding a 0.2-.mu.-thick **SiO2** film. By heating the crystal in a gas mixt. of 30 vol. % NH3 and 1 vol. % SiH4, a 0.1-.mu. thick Si3N4 film was formed on the **SiO2** layer. Photomasking and etching were applied to the crystal, and a **SiO2** layer partially covered with Si3N4 was obtained. The oxide layer with or without Si3N4 contained many surface charges but few surface states. Depending on the aftertreatment of the crystal, e.g., heating in pure N or O at 1000.degree. either dry or wet, the no. of surface states and (or) surface charges in the **SiO2** layer varied. In most cases, the aftertreatment did not influence the properties of the **SiO2** areas covered by Si3N4. In the other method, a protective Si3N4 layer was deposited on **SiO2** by reaction of a gas mixt. of 50 vol. % N2H4, 50 vol. % SiH4, and traces of Hg vapor in uv light. After photomasking and etching, a **SiO2** film partially covered with Si3N4 was obtained, having a few oxide charges and few surface states. With these methods it is possible to vary and control the charge content of **SiO2** layers, which in turn influences the elec. properties of the underlying semiconductor. Good performance of **transistors**, diodes, and **integrated circuits** can be guaranteed.
The patent contains further a detailed treatment of the influence of oxide charges and surface states on the elec. properties of various semiconducting devices, e.g. MOS **transistors**. The use of oxide layers with or without Si3N4 and their application for charge control in areas such as emitter-base or base-collector junctions of MOS **transistors** is described. Undesirable inversion channels in planar semiconducting devices can be eliminated by means of oxide layers with locally different properties.

L31 ANSWER 26 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1970:16726 HCAPLUS
DN 72:16726
TI Research for development of thin-film space-charge-limited triode devices
AU Aubuchon, Kenneth G.; Knoll, Peter; Zuleeg, Rainer
CS Appl. Solid State Res. Dep., Hughes Aircraft Co., Newport Beach, Calif., USA
SO NASA Contract. Rep. (1967), NASA-CR-86184, 74 pp. Avail.: CFSTI
From: Sci. Tech. Aerosp. Rep. 1969, 7(18), 3462
CODEN: NSCRAQ
DT Report
LA English
AB Si-on-sapphire space-charge-limited triodes were designed and fabricated. The Si films were grown on oriented sapphire **wafers** by the

pyrolysis of silane at 1000-1150.degree. and were investigated by x-ray diffraction methods and by Hall-effect measurements. The films with the best structural perfection, having hole mobilities of e ssentially **single-crystal** Si, were grown at 1050.degree.. Higher as well as lower pedestal temps. resulted in a poorer deposit. The high-temp. limitation for the film growth apparently is due to a chem. reaction between Si and sapphire which is enhanced with increasing temp . The max. frequency of oscillation obtained was 3-4 GHz for a source-drai n spacing of approx. 4 .mu.. Higher frequencies should be obtainable with further redn. in source-dra in spacing. Results of radiation tests with doses up to 2 .times. 105 rad s are presented, along with comparative tests on metal-nitride-semiconductor and metal-oxide-semiconductor capacitors which indicate that **Si nitride** is much less sensitive to ionizing radiation than **SiO2**.

L31 ANSWER 27 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1968:99887 HCAPLUS
DN 68:99887
TI Process for depositing **silicon nitride** layers on a substrate, especially to produce semiconductor devices
PA N. V. Philips' Gloeilampenfabrieken
SO Neth. Appl., 5 pp.
CODEN: NAXXAN
DT Patent
LA Dutch
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	NL 6606405		19671113	NL	19660511

AB Semiconductor devices such as planar **transistors**, field-effect **transistors** of metal-oxide-semiconductor type, and **integrated circuits** can be prepd. by depositing a compd. of near the stoichiometric compn. Si3N4 on substrates of Si, Ge, or AIIIBV compds. from a gas phase at 500-750.degree.. A special feature is that the gas phase contains neither H nor N excess above the active ingredients and the relatively low temp. of operation. A disk-shaped substrate 1 mm. thick and 10 mm. in diam. of **single-crystal** Si is heated in a **quartz** bulb in a vacuum to 600.degree., whereupon a mixt. of 1 part SiH4 and 2 parts NH3 by vol. is introduced at a total pressure of 10 mm. Hg at 25.degree.. The deposit of Si3N4 reaches a thickness of 0.1 .mu. in 30 min. On repeating the same expt. with a Ge disk of identical dimensions at 600.degree. in the evacuated **quartz** bulb and an atm. of 1 part SiH4 and 4 parts N2H4 by vol. at a total pressure of 10 mm. Hg at 25.degree., the Si3N4 deposit reaches 0.3 .mu. thickness in 30 min. It is desirable to be able to work at atm. pressure using a carrier gas under exclusion of H and N, which both produce side effects. A Ge disk of the same dimensions as before is heated to the reaction temp. in a **quartz** bulb with He at atm. pressure. Through 2 sep. inlet ducts, SiCl4 and N2H4, resp., are introduced into the vicinity of the substrate by means of a He stream at atm. pressure. The vol. ratio of SiCl4 to N2H4 is 1:4, and the partial pressures of the 2 compds. add up to 10 mm. Hg. Under these conditions, a deposit thickness of 1 .mu. Si3N4 is obtained in 30 min. Si3N4 is preferable to Si oxide layers because of its higher dielec. strength, better resistance to chem. attack, and smaller penetrability to diffusing doping agents, so that it masks better than the Si oxide generally used for such a purpose.

L31 ANSWER 28 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1967:109532 HCAPLUS
DN 66:109532

12/04/2002

TI Semiconductor **integrated circuit** structure
PA Signetics Corp.
SO Brit., 9 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 1061060		19670308		
PRAI	US		19631216		
	US		19640120		

AB A new and improved **integrated circuit** structure is described which can be utilized for isolating active and passive elements in integrated circuitry. The semiconductor structure is prepd. by forming an insulating layer (**SiO2**) on a slice or **wafer** of **single-crystal Si** (n- or p-type). A pattern of grooves is formed on the exposed **SiO2** layer by photolithographic techniques. The semiconductor structure, using the oxide layer as a mask, is etched until the pattern penetrates the **wafer** to a predetd. depth. The insulating layer is grown in the grooves by oxidn. A support structure, e.g. polycryst. Si, Al2O3, or **SiO2**, is deposited on the grid structure. Portions of the grid structure of the insulating material are lapped or etched to remove the bottom portion of the semiconductor structure. The grid structure forms islands of **single-crystal** Si embedded in the support structure and which are elec. isolated from each other by the grid structure. Active and passive elements are formed in the islands by use of conventional masking and diffusion techniques. Interconnecting contacts are provided by evapg. metal over the surface and then removing undesirable excess metal by photomasking techniques. A completed structure has active elements (**transistors**) and passive elements (diodes) formed in the islands and interconnected by evapd. metal leads and by thin-film resistors. It is preferred that the structure materials have the proper adherence qualities and thermal coeff. of expansion. The use of polycryst. Si as a support structure provides an elevated temp. capability without breaking or other adverse effects.

L31 ANSWER 29 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1967:15078 HCAPLUS
DN 66:15078
TI Semiconductor solid-state circuits
IN Horsley, Anthony W.
PA Standard Telephones and Cables Ltd.
SO Brit., 3 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 1045788		19661019	GB	19650930

AB A method of manufg. semiconductor solid-state circuits has been described. An accurately flat and parallel n-type **single-crystal** Si **wafer** .apprx.0.006 in. thick is taken. On one side of it, a 1-.mu. dielec. layer **SiN** is formed by vapor deposition. A polycryst. Si layer 0.008 in. thick is deposited over the dielec. layer to act as a rigid substrate for the completed device. This layer matches the coeff. of expansion of the Si **wafer**. To effect impurity diffusion, the Si **wafer** is then reduced to min. practicable thickness, 0.0005 in., by the air abrasion technique. A thermally grown

SiO2 layer on the **wafer** serves as a mask for the fabrication of **transistors** formed by successive p-type impurity diffusion by the photolithographic process. Each p-type layer contains a diffused n-type layer. Overall evapn. of an Al layer followed by selective removal of parts of the evapd. layer provides individual base contacts and interconnects the emitter of one **transistor** and the collector of the next. A photoresist layer is then formed over the device and exposed through a mask to get the necessary window pattern. Grooves are etched through the Si **wafer** down to the dielec. layer in a pattern corresponding to the windows. The photoresist layer is then removed.

L31 ANSWER 30 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1967:15077 HCAPLUS
DN 66:15077
TI Manufacture of semiconductor solid-state circuits
IN Horsley, Anthony W.
PA Standard Telephones and Cables Ltd.
SO Brit., 3 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 1045787		19661019	GB	19650930

AB A method of manufg. semiconductor solid-state circuits has been described. An accurately flat and parallel n-type **single-crystal** Si **wafer** .apprx.0.006 in. thick is taken. On one side of it, a dielec. layer of **SiN**, 1 .mu. thick, which is insol. in HF etches, is formed by vapor deposition. A polycryst. Si layer .apprx.0.008 in. thick is deposited over the dielec. layer to act as a rigid substrate for the completed device. This layer matches the coeff. of expansion of the Si **wafer**. To effect impurity diffusion, the Si **wafer** is reduced to min. practicable thickness 0.0005 in. by the air-abrasion technique. The **wafer** is then coated with a photoresist layer and exposed through a mask to give a desired pattern of windows. Grooves 0.002 in. wide are etched through the **wafer** and down to the dielec. layer. The exposed Si surfaces are passivated by a thermally grown **SiO2** layer to ensure high breakdown voltage. The **SiO2** layer serves as a masking layer for the fabrication of **transistors** in the spaces between the grooves through p-type impurity diffusion by the photolithographic process. Each p-type layer contains a diffused n-type layer. If the dielec. layer used is **SiO2**, which is sol. in HF etches, the grooves are etched down to the polycryst. substrate. Overall evapn. of an Al layer followed by selective removal of parts of the evapd. layer provides individual base contacts and interconnects the emitter of one **transistor** and the collector of the next.

L35 ANSWER 1 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:595271 HCAPLUS
DN 137:148779
TI SOI semiconductor **integrated circuit** for eliminating floating **body** effects in SOI MOSFETs, and method of fabricating the same
IN Lee, Soo-cheol; Lee, Tae-jung
PA Samsung Elecronics Co., Ltd., S. Korea
SO U.S. Pat. Appl. Publ., 23 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002105032	A1	20020808	US 2001-872429	20010601
	DE 10143256	A1	20020912	DE 2001-10143256	20010830
	JP 2002289873	A2	20021004	JP 2002-24111	20020131
PRAI	KR 2001-5976	A	20010207		

AB A silicon-on-insulator (SOI) **integrated circuit** and a method of fabricating the SOI **integrated circuit** are provided. A plurality of **transistor** active regions and at least one **body** contact active region are formed on an SOI substrate. A semiconductor residue layer, which is thinner than the **transistor** active regions and the **body** contact active region, is disposed between the **transistor** active regions and the **body** contact active region. The **transistor** active regions, the **body** contact active region and the semiconductor residue layer are disposed on a buried insulating layer of the SOI substrate. The semiconductor residue layer is covered with a partial trench isolation layer. The invention relates to a SOI MOSFET VLSI, wherein a bar-shaped full trench isolation layer is interposed between adjacent **transistor** active regions. The full trench isolation layer is in contact with sidewalls of the **transistor** active regions adjacent thereto and is in contact with the buried insulating layer between the adjacent **transistor** active regions. An insulated gate pattern crosses over the resp. **transistor** active regions. The insulated gate pattern is disposed to be parallel with the full trench isolation layer.

L35 ANSWER 2 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:595266 HCAPLUS
DN 137:148776
TI Structure and method for a compact trench-capacitor DRAM cell with **body** contact
IN Mandelman, Jack A.; Radens, Carl J.
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 26 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002105019	A1	20020808	US 2001-777576	20010205

AB A compact DRAM cell array that substantially minimizes floating-**body** effects and device-to-device interactions is disclosed. The compact DRAM cell array includes a plurality of annular memory cells that are arranged in rows and columns. Each annular memory cell includes a vertical MOSFET and an underlying capacitor that are in elec. contact to

each other through a buried-strap out-diffusion region which is present within a portion of a wall of each annular memory cell such that the portion partially encircles the wall. The remaining portions of the wall of each annular memory cell have a **body** contact region that serves to elec. connect the annular memory cell to an adjacent array well region. The DRAM cell array also includes a plurality of word lines overlaying the vertical MOSFETs, and a plurality of bit lines that are orthogonal to the plurality of word lines.

L35 ANSWER 3 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:466473 HCAPLUS
DN 137:27013
TI **Transistor** and **logic circuit** on thin silicon-on-insulator **wafers** based on gate induced drain leakage currents
IN Chi, Min-hwa
PA Taiwan
SO U.S. Pat. Appl. Publ., 15 pp., Division of U.S. Ser. No. 737,946. CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002074599	A1	20020620	US 2001-865929	20010524
PRAI	US 2000-737946	A3	20001218		

AB The invention relates to semiconductor inverter for NAND **logic circuits**, wherein the **transistor** structure is fabricated on thin SOI **wafer**. The **transistor** on thin SOI has gated n+ and p+ junctions, which serve as switches turning on and off GIDL current on the surface of the junction. GIDL current will flow into the floating **body** and clamp its potential and can thus serve as an output node. The **transistor** can function as an inverter. The **body** (either n-well or p-well) is isolated from the n+ or P+ "GIDL switches" by a region of opposite doping type, i.e., p-base and n-base. The basic building blocks of **logic circuits**, e.g., NAND and NOR gates, are easily implemented with such **transistors** on thin SOI **wafers**. These new **transistors** on thin SOI only need contacts and metal line connections on the Vcc and Vss . The connection of fan-outs (between the output and input) can be implemented by capacitor coupling. The **transistor** structure and operation is useful for high-performance, low-voltage, and low-power VLSI circuits on SOI **wafers**.

L35 ANSWER 4 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:763499 HCAPLUS
DN 135:297131
TI SOI semiconductor **integrated circuit** for eliminating floating **body** effects in SOI MOSFETs and method of fabricating the same
IN Kim, Young-wug; Kim, Byung-sun; Kang, Hee-sung; Ko, Young-gun; Park, Sung-dae; Kim, Min-su; Kim, Kwang-il
PA Samsung Electronics,co. Ltd, S. Korea
SO U.S. Pat. Appl. Publ., 33 pp., Cont.-in-part of U.S. Ser. No. 695,341. CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001031518	A1	20011018	US 2001-782116	20010213

PRAI US 1999-161479P P 19991025
US 2000-695341 A2 20001024

AB A Si-on-insulator (SOI) **integrated circuit** and a method of fabricating the SOI **integrated circuit** are provided. At least 1 isolated **transistor** active region and a **body** line are formed on an SOI substrate. The **transistor** active region and the **body** line are surrounded by an isolation layer which is in contact with a buried insulating layer of the SOI substrate. A portion of the sidewall of the **transistor** active region is extended to the **body** line. Thus, the **transistor** active region is elec. connected to the **body** line through a **body** extension. The **body** extension is covered with a **body** insulating layer. An insulated gate pattern is formed over the **transistor** active region, and 1 end of the gate pattern is overlapped with the **body** insulating layer.

L35 ANSWER 5 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:560102 HCAPLUS
DN 135:115638
TI Silicon-on-insulator field effect **transistor** with improved **body** ties for rad-hard applications
IN Schwank, James R.; Shaneyfelt, Marty R.; Draper, Bruce L.; Dodd, Paul E.
PA Sandia Corp., USA
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6268630	B1	20010731	US 1999-270374	19990316

AB A Si-on-insulator (SOI) field-effect **transistor** (FET) and a method for making the same are disclosed. The SOI FET was characterized by a source which extends only partially (e.g. about half-way) through the active layer wherein the **transistor** is formed. Addnl., a minimal-area **body** tie contact is provided with a short-circuit elec. connection to the source for reducing floating **body** effects. The **body** tie contact improves the elec. characteristics of the **transistor** and also provides an improved single-event-upset (SEU) radiation hardness of the device for terrestrial and space applications. The SOI FET also provides an improvement in total-dose radiation hardness as compared to conventional SOI **transistors** fabricated without a specially prepd. hardened buried oxide layer. Complementary n-channel and p-channel SOI FETs can be fabricated according to the present invention to form **integrated circuits** (**ICs**) for com. and military applications.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 6 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:488954 HCAPLUS
DN 135:85557
TI Fabrication of high withstand-voltage and low ON-resistance DMOS **transistors** for monolithic **ICs**
IN Sato, Akira
PA Seiko Epson Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001185724	A2	20010706	JP 1999-367014	19991224

AB The title fabrication involves (1) forming an n--drift region on a Si substrate, (2) patterning a selective-oxidn. mask on the substrate, (3) selectively oxidizing to give a component-isolation insulator film, (4) lithog. processing the mask layer to be selectively etched according to its resist so as to be provided as a p+-**body** diffusion layer and as a doping mask over an n--source offset layer, and (5) subsequently continuing fabrication processes same as those for fabrication of MOS **transistor** thereafter. The fabrication process provides decreased process steps and consequently saving manufg. cost.

L35 ANSWER 7 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:331359 HCAPLUS
DN 134:335237
TI Field effect **transistor** with non-floating **body** and method for forming same on a bulk silicon **wafer**
IN Ju, Dong-Hyuk
PA Advanced Micro Devices, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6229187	B1	20010508	US 1999-420972	19991020
	US 6465852	B1	20021015	US 2000-633960	20000808
PRAI	US 1999-420972	A2	19991020		

AB A Si on insulator (SOI) **wafer** is formed with an unoxidized perforation in the insulating **SiO_2** buried oxide layer. A field effect **transistor** (FET) structure on the SOI **wafer** is located above the unoxidized perforation such that the unoxidized perforation provides for elec. coupling between the channel region of the FET with the bulk Si substrate to eliminate the floating **body** effect caused by charge accumulation in the channel regions due to historical operation of the FET. The method of forming the FET includes masking a Si **wafer** prior to an O implantation process to form the unoxidized perforated buried oxide layer in the **wafer**.
RE.CNT 30 THERE ARE 30 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 8 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:137515 HCAPLUS
DN 134:171925
TI Method of simultaneously growing oxide layers with different thicknesses on a semiconductor **body** using selective implantations of oxygen and nitrogen
IN Lin, Chuan
PA Infineon Technologies North America Corp., USA
SO PCT Int. Appl., 26 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001013421	A1	20010222	WO 2000-US22191	20000814

W: CN, JP, KR
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL,

PT, SE
PRAI US 1999-375764 A 19990818
AB A method for controlling gate oxide thicknesses in either dual or triple gate oxide arrays uses ion implantation of both relatively low doses of O into some portions and relatively low doses of N into other portions of the surface of a Si **wafer**. Gate oxide layers are all thermally grown simultaneously. For dual gate oxide arrays the method produces thick and thin gate oxide layers, resp., during a single thermal growth step, with resulting wider processing windows and better device reliability. An intermediate oxide thickness, useful for triple gate oxide arrays, can be thermally grown in the nonimplanted portions of the major surface simultaneously with the growth of all other oxide layers.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 9 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:382083 HCAPLUS
DN 132:355701
TI Manufacturing method of SOI semiconductor device
IN Kim, Won-chol; Jong, Un-sung
PA Samsung Electronics Co., Ltd., S. Korea
SO Repub. Korea, No pp. given
CODEN: KRXXFC
DT Patent
LA Korean
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	KR 9500106	B1	19950109	KR 1992-160	19920108

AB The method for forming a field oxide film on the SOI for the active region isolation includes the steps of forming a pad oxide film (13) and a nitride film (14) on the SOI substrate (11) with a buried oxide layer (12), etching the films (14,13) of the thick oxide layer formation portion to form a thick field oxide film (15) by a 1st oxidn. process, etching the films (14,13) of the thin oxide layer formation portion to form a thin field oxide film (15') and a thick field oxide film (16) by a 2nd oxidn. process, and removing the films (14,13), thereby obtaining the thin and thick field oxide films on the SOI **wafer** to manuf. a **transistor** with a **body** node and a punch-through **transistor** on a SOI substrate.

L35 ANSWER 10 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:748263 HCAPLUS
DN 131:345323
TI Semiconductor device having dual gate and fabrication of same
IN Holloway, Thomas C.; Hattangady, Sunil V.
PA Texas Instruments Incorporated, USA
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5989962	A	19991123	US 1998-159040	19980923
PRAI	US 1997-60121P	P	19970926		

AB The invention comprises a method of forming a semiconductor device is provided where a first gate insulator layer is formed on an outer surface of semiconductor substrate. A mask **body** is formed to cover portions of the insulator layer. The exposed portions of the layer are subjected to a nitridation process to form a nitride layer. A second

oxidn. process forms a thick gate oxide layer. The nitride layer inhibits the growth of oxide resulting in a single integrated device having gate insulator layers having two different thicknesses such that high voltage and low voltage **transistors** can be formed on the same **integrated circuit**.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 11 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:588239 HCAPLUS
DN 131:222062
TI Insulated-gate field-effect semiconductor device and fabrication thereof
IN Hsu, Louis Lu Chen; Mandelman, Jack A.
PA International Business Machines Corp., USA
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11251579	A2	19990917	JP 1999-5079	19990112
	JP 3309078	B2	20020729		
	US 6177299	B1	20010123	US 1998-7908	19980115
	TW 429628	B	20010411	TW 1999-88100360	19990112
PRAI	US 1998-7908	A	19980115		

AB The invention relates to an insulated-gate field-effect semiconductor device, i.e., a SOI MOSFET LSI, wherein the field-effect **transistor body** is substantially isolated from the substrate except at the neck region that allows charge carrier exchange.

L35 ANSWER 12 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:417433 HCAPLUS
DN 131:52729
TI Method of forming vertical trench-gate semiconductor devices having self-aligned source and **body** regions
IN Choi, Yong-Cheol; Jeon, Chang-Ki
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5918114	A	19990629	US 1997-855459	19970513

AB Methods of forming vertical trench-gate semiconductor devices include the steps of patterning an oxidn. resistant layer having an opening therein, on a face of a semiconductor substrate, and then forming a trench in the semiconductor substrate, opposite the opening in the oxidn. resistant layer. An insulated gate electrode is then formed in the trench. The face of the semiconductor substrate is then oxidized to define self-aligned elec. insulating regions in the opening and at a periphery of the patterned oxidn. resistant layer. Here, the patterned oxidn. resistant layer is used as an oxidn. mask so that portions of the substrate underlying the oxidn. resistant layer are not substantially oxidized. Source and **body** region dopants of first and second cond. type, resp., are then implanted into the substrate to define preliminary source and **body** regions which extend adjacent a sidewall of the trench. During the implanting step, the elec. insulating regions are used as a self-aligned implant mask. The implanted dopants

are then diffused into the substrate to define source and **body** regions adjacent upper and intermediate portions of the sidewall of the trench, resp.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 13 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:300493 HCAPLUS
DN 129:11682
TI Fabrication of semiconductor device having semiconductor substrate formed using a porous semiconductor layer, and semiconductor device
IN Yonehara, Takao; Sato, Nobuhiko; et al.
PA Canon Kabushiki Kaisha, Japan
SO U.S., 88 pp., Cont.-in-part of U.S. Ser. No. 551,450, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 5

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5750000	A	19980512	US 1996-755356	19961125
	JP 05036915	A2	19930212	JP 1991-210369	19910729
	JP 3098810	B2	20001016		
	JP 05036916	A2	19930212	JP 1991-210370	19910729
	JP 3098811	B2	20001016		
	JP 05036714	A2	19930212	JP 1991-214241	19910801
	JP 3128076	B2	20010129		
	JP 05036953	A2	19930212	JP 1991-214243	19910801
	JP 3112102	B2	20001127		
	JP 05036954	A2	19930212	JP 1991-214244	19910801
	JP 3112103	B2	20001127		
	JP 05067627	A2	19930319	JP 1991-214242	19910801
	JP 3128077	B2	20010129		
	JP 05041488	A2	19930219	JP 1991-216573	19910802
	JP 3088032	B2	20000918		
	JP 05041489	A2	19930219	JP 1991-216574	19910802
	JP 3088033	B2	20000918		
	JP 05041505	A2	19930219	JP 1991-216575	19910802
	JP 3098815	B2	20001016		
	JP 09121039	A2	19970506	JP 1996-285165	19910802
	US 5371037	A	19941206	US 1991-740439	19910805
	US 6150031	A	20001121	US 1996-766888	19961213
PRAI	JP 1990-206548	A	19900803		
	JP 1991-210369	A	19910729		
	JP 1991-210370	A	19910729		
	JP 1991-214241	A	19910801		
	JP 1991-214242	A	19910801		
	JP 1991-214243	A	19910801		
	JP 1991-214244	A	19910801		
	JP 1991-216573	A	19910802		
	JP 1991-216574	A	19910802		
	JP 1991-216575	A	19910802		
	US 1991-740439	A2	19910805		
	US 1992-921232	B1	19920729		
	US 1994-191767	B1	19940204		
	US 1994-355117	B1	19941213		
	US 1995-514984	B3	19950814		
	US 1995-551450	B1	19951101		
	JP 1991-194138	A3	19910802		
	US 1994-297916	B1	19940831		
	US 1995-562644	B1	19951127		

AB A semiconductor device having a substrate with an insulating surface and a non-porous semiconductor region bonded to the **body** of the device. A porous semiconductor region on the surface of the substrate was removed by etching.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 14 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:115634 HCAPLUS
DN 128:161829
TI Semiconductor **IC** apparatus
IN Ueda, Kimihiro
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 24 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10041406	A2	19980213	JP 1996-189268	19960718

AB The invention relates to a MOS semiconductor **IC** app., e.g., a MOS **transistor** memory gate array **IC chip**, wherein the **body** terminal voltage of MOS **transistor** is controlled individually, to circumvent the limitation of the source voltage.

L35 ANSWER 15 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:635156 HCAPLUS
DN 125:263281
TI Manufacture of **integrated circuits** comprising lateral low- and high-voltage DMOS power devices and nonvolatile memory cells
IN Contiero, Claudio; Galbiati, Paola; Palmieri, Michele
PA Sgs-Thomson Microelectronics S.R.L., Italy
SO Eur. Pat. Appl., 18 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 731504	A1	19960911	EP 1995-830088	19950309
	R: DE, FR, GB, IT				
	US 6022778	A	20000208	US 1996-612722	19960308
	JP 08321556	A2	19961203	JP 1996-53114	19960311
	JP 2987098	B2	19991206		
PRAI	EP 1995-830088		19950309		

AB The process includes: forming resp. laterally displaced isolated semiconductor regions elec. insulated from each other and from a common semiconductor substrate, inside which the devices will be formed; forming conductive insulated gate regions for the lateral DMOS power devices and for the memory cells over the resp. isolated semiconductor regions; inside the isolated semiconductor regions for the lateral DMOS power devices, forming deep **body** regions aligned with the edges of the insulated gate regions, and channel regions extending under the insulated gate regions. The deep **body** regions are formed by means of a 1st implantation of a 1st dopant in a direction substantially orthogonal to the top surface of the **integrated circuit**, performed with an energy and with a dopant dose such that the concn. of the 1st dopant has a peak located at a prescribed distance from the surface of the isolated semiconductor regions. The channel regions are

formed by means of a 2nd implantation of a 2nd dopant along directions tilted at a prescribed angle with respect to the direction orthogonal to the top surface of the **integrated circuit**, in a dose and with an energy such that the channel regions are formed directly after the implantation of the 2nd dopant without performing a thermal diffusion of the 2nd dopant at a high temp.

L35 ANSWER 16 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1976:37947 HCAPLUS
DN 84:37947
TI Increasing the dopant level in a semiconductor region of a semiconductor **body** under an insulation layer
IN Stein, Karl Ulrich; Goser, Karl; Eichhorn, Juergen
PA Siemens A.-G., Ger.
SO Ger. Offen., 10 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 2424164	A1	19751127	DE 1974-2424164	19740517
	DE 2424164	B2	19791031		
	DE 2424164	C3	19800724		

AB The dopant concn. in certain regions of a semiconductor substrate is increased by forming an insulating layer (Si_3N_4) on the substrate, removing parts of the layer, forming another doped insulator layer (**SiO_2**) on the exposed portions of the substrate, and diffusing the dopants into the substrate during subsequent heat treatment. This method makes it possible to prep. integrated MOS devices with high thick-oxide starting voltages, small leakage currents, low diffusion capacitances, and low **transistor** starting voltages. The method requires no addnl. diffused regions, e.g. guard rings, or their assocd. masking and diffusion steps and does not increase the area of the **integrated circuit**.

12/04/2002

L49 ANSWER 1 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:676458 HCAPLUS
DN 137:178079
TI Method of manufacturing **transistor** having metal gate electrode in integratd circuit
IN Shih, Jiaw-Ren; Chen, Shui-Hung; Lee, Jian-Hsing
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO Taiwan, 20 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 406314	B	20000921	TW 1999-88106714	19990427

AB The method comprises the following steps: providing a semiconductor substrate and forming a mask layer, and then defining the mask layer to the semiconductor substrate to form a ditch, defining the scope of the metal gate electrode of the **transistor**, forming the metal gate electrode of the **transistor**, and then after forming a gate dielec. layer in the ditch, forming the metal gate electrode of the **transistor** on the gate dielec. layer, and forming drain and **source areas** on the semiconductor substrate at both sides of the metal gate electrode and hence a **transistor** is formed.

L49 ANSWER 2 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:616100 HCAPLUS
DN 137:162430
TI Pull-down **transistor**
IN Pai, Chi-horn; Hsiao, Chih-yuan
PA Taiwan
SO U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002109174	A1	20020815	US 2001-783846	20010215

AB The present invention provides an asym. pull-down **transistor** in a semiconductor device. The **transistor** comprises a substrate, a drain region in the substrate, a **source region** in the substrate wherein the **source region** is spaced from the drain region by a channel region and extended into a portion of the channel region, a gate structure above the channel region, and a spacer at a sidewall of the gate structure. A method comprises providing a substrate, forming a gate structure on the substrate, forming a mask covering the partial gate structure and the partial substrate. Next, the gate structure and the mask are used as implanting mask and the first ions are tilted implanted into the substrate to form a **source region** and a drain region. The **source region** is extended into the partial channel. Then the mask is removed and a spacer is formed at a sidewall of the gate structure.

L49 ANSWER 3 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:616091 HCAPLUS
DN 137:162425
TI DRAM cell and method of manufacturing the same

IN Shin, Chul-ho; Chi, Kyeong-koo
PA S. Korea
SO U.S. Pat. Appl. Publ., 20 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002109155	A1	20020815	US 2002-38911	20020108
	JP 2002280462	A2	20020927	JP 2002-30888	20020207
PRAI	KR 2001-6408	A	20010209		

AB The invention relates to a process for making a DRAM cell, comprising forming an isolation layer on a given region of a substrate to define an active region having a plurality of line shaped sub-regions; forming at least a pair of cell **transistors** in each line shaped sub-region, each cell **transistor** of a pair having a common drain region and resp. **source regions**; forming a bit line pad on each common drain region and a storage node pad on each **source region**; forming a bit line pad protecting layer pattern having portions parallel to the word line, that covers the bit line pad; and forming storage nodes on storage node pads. The storage nodes of the DRAM cell contact with the storage node pads and are insulated elec. from the bit line pad by the bit line pad protecting layer pattern.

L49 ANSWER 4 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:540074 HCAPLUS
DN 137:87101
TI Split gate field effect **transistor** (FET) device employing dielectric barrier layer and method for fabrication thereof
IN Hsieh, Chia-Ta; Kuo, Di-Son; Yeh, Jake; Chang, Chuan-Li; Chu, Wen-Ting; Tsaur, Sheng-Wei
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002093044	A1	20020718	US 2001-761276	20010116
	US 6468863	B2	20021022		

AB Within both a method for fabricating a split gate field effect **transistor** and the split gate field effect **transistor** fabricated employing the method, there is employed a patterned **silicon nitride** barrier dielec. layer formed covering a first portion of a floating gate and a first portion of a semiconductor substrate adjacent the first portion of the floating gate. Within the first portion of the semiconductor substrate there is eventually formed a source/drain region, and more particularly a **source region**, when fabricating the split gate field effect **transistor**. The patterned **silicon nitride** barrier dielec. layer inhibits when fabricating the split gate field effect **transistor** ion implant damage of the floating gate and oxidative loss of a floating gate electrode edge.

L49 ANSWER 5 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:522568 HCAPLUS
DN 137:87030
TI Aluminum nitride and aluminum oxide/aluminum nitride heterostructure gate dielectric stack based field effect **transistors** and method for

forming same
IN Bojarczuk, Nestor A.; Cartier, Eduard; Guha, Supratik; Ragnarsson, Lars-ake
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002090773	A1	20020711	US 2001-755164	20010108
	JP 2002246594	A2	20020830	JP 2001-388832	20011221
	CN 1363958	A	20020814	CN 2001-130281	20011229
PRAI	US 2001-755164	A	20010108		

AB A structure (e.g., field effect **transistor**) and a method for making the structure, include a substrate having a **source region**, a drain region, and a channel region, an insulating layer disposed over the channel region, the insulating layer including a layer including aluminum nitride disposed over the channel region, and a gate electrode disposed over the insulating layer.

L49 ANSWER 6 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:487984 HCAPLUS
DN 137:40410
TI Metal-oxide-semiconductor **transistor** structure and method of manufacturing same
IN Hower, Philip L.; Wofford, Larry
PA USA
SO U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002079514	A1	20020627	US 2001-61140	20011025
PRAI	US 2000-258892P	P	20001227		

AB The invention relates to a process for making a metal-oxide-semiconductor **transistor** structure, comprising forming dielec. isolation regions in a semiconductor substrate, forming a first dielec. layer outwardly from the semiconductor substrate, forming a polysilicon layer outwardly from the first dielec. layer, etching a portion of the polysilicon layer to form a gate, and forming at least one notch in a first side of the gate. The method further includes etching a portion of the first dielec. layer to expose the semiconductor substrate, forming an n+ **source region** in the semiconductor substrate adjacent the first side of the gate, forming an n+ drain region in the semiconductor substrate adjacent a second side of the gate, and forming at least one p+ substrate contact region proximate the notch and adjacent the n+ **source region**.

L49 ANSWER 7 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:461262 HCAPLUS
DN 137:26934
TI Fabrication of wide metal silicide on narrow polysilicon gate structure of MOSFET
IN Yu, Bin
PA Advanced Micro Devices, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM

DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6406986	B1	20020618	US 2000-603046	20000626
	US 6326291	B1	20011204	US 2001-808839	20010315
PRAI	US 2000-603046	A2	20000626		

AB A MOSFET has a drain region, a **source region**, and a channel region, and the MOSFET initially has a gate comprised of a capping layer on a polysilicon structure disposed on a gate dielec. over the channel region. A drain silicide and a source silicide having a first silicide thickness are formed in the drain region and the **source region**, resp. A dielec. layer is deposited over the drain region, the **source region**, and the gate. The dielec. layer is polished until the capping layer of the gate is exposed such that the capping layer and the first dielec. layer are substantially level. The capping layer on the polysilicon structure of the gate is etched away such that the top of the polysilicon structure is exposed. A top portion of the first dielec. layer is etched away until sidewalls at a top portion of the polysilicon structure are exposed. A polysilicon spacer is formed at the exposed sidewalls at the top portion of the polysilicon structure. A silicidation metal is deposited on the top of the polysilicon structure that is exposed and on the polysilicon spacer. A silicidation anneal is performed with the silicidation metal and the polysilicon structure that is exposed and the polysilicon spacer to form a gate silicide having a second silicide thickness on top of the polysilicon structure of the gate. Because the gate silicide is formed with the added polysilicon spacer at the exposed sidewalls of the polysilicon structure, the gate silicide has a width that is larger than a width of the polysilicon structure of the gate. In addn., the gate silicide is formed in a sep. step from the step for forming the drain silicide and the source silicide such that the gate silicide may have a larger thickness and be comprised of different metal silicide material from that of the drain silicide and the source silicide.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L49 ANSWER 8 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:387644 HCAPLUS
DN 136:394306
TI High-voltage metal-oxide-semiconductor **transistor** fabrication
IN Tung, Ming-Tsung
PA United Microelectronics Corp., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6392274	B1	20020521	US 2000-542842	20000404

AB A method for fabricating an HVMOS **transistor** that can reduce snapback is disclosed. The semiconductor **wafer** comprises an N-type Si substrate, and a P-type epitaxial layer formed on the surface of the Si substrate. The HVMOS **transistor** comprises a 1st P-well region formed within the epitaxial layer, a 2nd P-well region formed within the 1st P-well region a **source region** formed within the 2nd P-well region, an N-drain region formed in the epitaxial layer, a gate, and an N-type diffused region formed both in the epitaxial layer and in the Si substrate. The diffused region is under the 1st P-well region and overlaps the 1st P-well region.

12/04/2002

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RE.CNT  10     THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT

L49  ANSWER 9 OF 21  HCAPLUS  COPYRIGHT 2002 ACS
AN   2002:346001  HCAPLUS
DN   136:362554
TI   DRAM memory cell and array having pass transistors with recessed
     channels
IN   Walker, Darryl
PA   Texas Instruments, Inc., USA
SO   U.S., 14 pp.
     CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.        KIND  DATE           APPLICATION NO.  DATE
     ---------------   ----  --------       ---------------  --------
PI   US 6384439        B1    20020507       US 1999-241267   19990201
PRAI US 1998-73327P    P     19980202
AB   A dynamic random access memory (DRAM) cell and assocd. array are
     disclosed.  In a first embodiment, the DRAM cell includes a storage
     capacitor and a pass transistor.  The pass transistor
     is formed within a silicon mesa, and includes a source
     region, drain region and channel region.  The channel region is
     formed below a furrow that is inset with respect to the top surface of the
     silicon mesa.  The channel region has a smaller thickness than that of the
     source region and drain region.  A top gate is disposed
     over the channel region.  Due to the reduced thickness channel region,
     greater control of the operation of the pass transistor is
     provided, including an off state with reduced source-to-drain leakage.
     The greater thickness of the source region and drain
     region (relative to the channel region) provides greater immunity to the
     adverse effects of contact spiking.
RE.CNT  6      THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT

L49  ANSWER 10 OF 21  HCAPLUS  COPYRIGHT 2002 ACS
AN   2002:143253  HCAPLUS
DN   136:192782
TI   Method of making ultra-thin oxide formation using selective etchback
     technique integrated with thin nitride layer for high performance MOSFET
IN   Gardner, Mark I.; Allen, Michael; Fulford, H. Jim
PA   Advanced Micro Devices, Inc., USA
SO   U.S. Pat. Appl. Publ., 12 pp.
     CODEN: USXXCO
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.        KIND  DATE           APPLICATION NO.  DATE
     ---------------   ----  --------       ---------------  --------
PI   US 2002022325     A1    20020221       US 1998-2724     19980105
AB   A semiconductor device having gate oxide with a 1st thickness and a 2nd
     thickness is formed by initially implanting a portion of the gate area of
     the semiconductor substrate with N ions and then forming a gate oxide on
     the gate area.  Preferably the gate oxide is grown by exposing the gate
     area to an environment of O2.  A N implant inhibits the rate of
     SiO2 growth in an O2 environment.  Therefore, the portion of the
     gate area with implanted N atoms will grow or form a layer of gate oxide,
     such as SiO2, which is thinner than the portion of the gate area
     less heavily implanted or not implanted with N atoms.  The gate oxide
     layer could be deposited rather than growing the gate oxide layer.  After
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forming the gate oxide layer, polysilicon is deposited onto the gate oxide. The semiconductor substrate can then be implanted to form doped drain and **source regions**. Spacers can then be placed over the drain and **source regions** and adjacent the ends of the sidewalls of the gate.

L49 ANSWER 11 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:546086 HCAPLUS
DN 135:115605
TI Design and fabrication of a sub-micron MOS **transistor**
IN Ma, Yanjun; Evans, David Russell; Ono, Yoshi; Hsu, Sheng Teng
PA USA
SO U.S. Pat. Appl. Publ., 7 pp., Cont.-in-part of U.S. Ser. No. 4,991.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001009784	A1	20010726	US 2001-783760	20010214
	US 6274421	B1	20010814	US 1998-4991	19980109
	JP 11224949	A2	19990817	JP 1998-336093	19981126
	TW 434901	B	20010516	TW 1998-87120673	19981211
PRAI	US 1998-4991	A2	19980109		

AB A method of fabricating a sub-micron MOS **transistor** includes prepg. a substrate, including isolating an active region therein; depositing a gate oxide layer; depositing a 1st selective etchable layer over the gate oxide layer; depositing a 2nd selective etchable layer over the 1st selective etchable layer; etching the structure to undercut the 1st selective etchable layer; implanting ions in the active region to form a **source region** and a drain region; depositing and planarizing the oxide; removing the remaining 1st selective etchable layer and the 2nd selective etchable layer; depositing a gate electrode; and depositing oxide and metalizing the structure. A sub-micron MOS **transistor** includes a substrate; and an active region, including a gate region having a length of <1 .mu.m; a **source region** including a lightly-doped drain (LDD) **source region**; and a drain region including a LDD drain region.

L49 ANSWER 12 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:134148 HCAPLUS
DN 134:201510
TI MOS **transistor** and fabrication thereof
IN Oki, Ichiro
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001053280	A2	20010223	JP 1999-224067	19990806

AB The invention relates to a MOS **transistor integrated circuit**, i.e., a SOI-structure CMOS LSI, wherein the extended source layout minimizes junction leaks caused by the presence of lattice defect layer in the **source region**.

L49 ANSWER 13 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:31112 HCAPLUS
DN 134:94350

TI Semiconductor device and fabrication of same.
IN Morikawa, Takashi
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001007218	A2	20010112	JP 1999-173538	19990621

AB The fabrication process includes forming metal layers capable of forming elec. conductive compds. with a semiconductor (e.g., Si) on a semiconductor substrate having diffusion **regions** (**source** /drain diffusion layers), conductor regions (gate electrode) and insulator regions (element-sepn. regions, side wall insulator layers) formed thereon, introducing Si into desired regions of the metal layers for forming 1st, 2nd and 3rd elec. conductive compd. layers for connecting source/drain diffusion layers with gate wiring by reacting metal layers with Si, simultaneously forming elec. conductive layers on source/drain diffusion layers and gate electrodes, and then removing unreacted metal layers. The 1st, 2nd and 3rd elec. conductive compd. layers are Co silicide or Ti silicide layers.

L49 ANSWER 14 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:618442 HCAPLUS
DN 129:253488
TI Memory cell structure fabricated by forming a dielectric layer directly on an insulated surface of a substrate
IN Ling, Peiching
PA Advanced Materials Engineering Research, Inc., USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5811852	A	19980922	US 1996-587952	19960117

AB A PROM includes a **transistor** region in a substrate including a **source region**, a drain region, and a floating gate region disposed between the drain and **source regions**. The PROM further includes a floating gate formed on top of the floating gate region with a single polysilicon layer on the substrate. The PROM further includes a floating gate extension region disposed near the **transistor** region and connected to the floating gate region. The PROM further includes a control gate formed on the substrate near the floating gate extension region opposite the **transistor** region, whereby the charge state of the floating gate extension region is controlled by the control gate. The PROM may include an embedded DRAM on the same **chip**.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L49 ANSWER 15 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:398065 HCAPLUS
DN 129:102946
TI Semiconductor device and fabrication thereof
IN Ando, Yuichi
PA Ricoh Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10163338	A2	19980619	JP 1996-334786	19961128

AB The invention relates to a semiconductor device, esp., a MOS **transistor** LSI, monolithically integrating a high voltage MOS **transistor** and a low voltage MOS **transistor**, wherein the LDD **structure source**-drain maximizes hot carrier breakdown voltage.

L49 ANSWER 16 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:527859 HCAPLUS
DN 127:228350
TI Nanofabrication in manufacture of **transistor**
IN Yamanaka, Eiji
PA Tokin Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09205216	A2	19970805	JP 1996-10171	19960124

AB The invention relates to a process for making a **transistor**, esp., static induction **transistor**, for high-frequency operation, wherein the **source region** and the gate region is formed through microwindows in the surface of the **wafer**.

L49 ANSWER 17 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:643526 HCAPLUS
DN 121:243526
TI In-plane-gate (IPG) **transistors, integrated circuits** containing them, and their production
IN Hosogi, Kenji
PA Mitsubishi Denki Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 46 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 603711	A2	19940629	EP 1993-120125	19931214
	R: DE, FR, GB				
	JP 06244216	A2	19940902	JP 1993-128623	19930531
	US 5449929	A	19950912	US 1993-169141	19931220
PRAI	JP 1992-356619		19921221		
	JP 1993-128623		19930531		

AB The prodn. of an IPG **transistor** comprises: producing a channel portion in which a quasi-1-dimensional conductive channel elec. connecting a **source region** and a drain region is generated, on a substrate; and producing gate portions, each portion including a gate electrode layer for controlling generation and forfeiture of the channel, so that the upper surfaces of the gate layer and the channel are substantially in the same plane. In prodn. of the gate portions, gaps between the channel portion and the gate portions are regulated by side walls produced self-alignedly on the side wall surfaces of the channel

portion. Thus, gap grooves of a high aspect ratio can be produced between the channel portion and the gate portion without being restricted by the dry etching technique.

L49 ANSWER 18 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:548261 HCAPLUS
DN 115:148261
TI MIS-type field-effect **transistors**
IN Takada, Ryoji
PA Seiko Epson Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03057278	A2	19910312	JP 1989-193487	19890725

AB The title **transistor** comprises (1) a 1st cond.-type highly doped **source region** formed on the surface of a 2nd cond.-type semiconductor substrate, (2) a gate insulator film formed adjacent to the **source region**, (3) a gate contact formed on the gate insulator film, (4) a sepn. insulator film whose thickness is thicker than that of the gate insulator film and which is formed apart from the **source region**, (5) a 1st cond.-type lightly doped 1st drain region provided in self-alignment below the sepn. insulator film, (6) a highly doped 2nd drain region provided in adjacent to the 1st drain region, and (7) a 2nd cond.-type doped region which is doped in self-alignment in the **source region** at a higher dopant concn. than that of the semiconductor substrate. The title **transistor** for **integrated circuits** with high-withstand voltage has an increased operational capability owing to its decreased **source region** area, its decreased ON-resistance, and also its decreased effective channel length.

L49 ANSWER 19 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1975:420800 HCAPLUS
DN 83:20800
TI **Integrated circuit** components having a field-effect **transistor** with insulated gate electrode
IN Dingwall, Andrew G. F.
PA RCA Corp., USA
SO Ger. Offen., 25 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 2436486	A1	19750220	DE 1974-2436486	19740729
	US 3888706	A	19750610	US 1973-385668	19730806
	IT 1015393	A	19770510	IT 1974-24413	19740625
	CA 1012657	A1	19770621	CA 1974-204726	19740715
	GB 1471355	A	19770427	GB 1974-33314	19740729
	NL 7410215	A	19750210	NL 1974-10215	19740730
	BR 7406237	A0	19750527	BR 1974-6237	19740730
	AU 7471922	A1	19760205	AU 1974-71922	19740801
	SE 7410035	A	19750207	SE 1974-10035	19740805
	SE 393221	B	19770502		
	FR 2240527	A1	19750307	FR 1974-27141	19740805
	FR 2240527	B1	19781124		

	BE 818546	A1	19741202	BE 1974-147340	19740806
	JP 50046082	A2	19750424	JP 1974-90664	19740806
	JP 52023231	B4	19770622		
PRAI	US 1973-385668		19730806		

AB A metal-oxide-silicon field-effect **transistor** (MOSFET) of p or n type is formed on a Si **wafer** in a single diffusion step. The square frame-like mask is built up of 3 layers: **SiO2** gate insulation 1000 .ANG. thick which is formed by thermal oxidn., polycryst. heat-resistant conductive Si 3000-6000 .ANG. which is formed by pyrolytic decompn. of SiH4, and Si3N4 insulation which is deposited from SiH4 and NH3 at 1000.degree.. The 2 square windows obtained from photoresists and etching are used for the diffusion step to form the drain and **source areas**. Finally, Al electrodes and conducting strips are applied.

L49 ANSWER 20 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1973:519777 HCAPLUS
DN 79:119777
TI Semiconductor devices
IN Boleky, Edward J., III
PA RCA Corp.
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 3745647	A	19730717	US 1970-78806	19701007
	GB 1332384	A	19731003	GB 1971-28758	19710618
	FR 2112263	A5	19720616	FR 1971-24443	19710705
	FR 2112263	B1	19770603		
	JP 50010102	B4	19750418	JP 1971-49885	19710706
PRAI	US 1970-78806		19701007		

AB A process is given for sealing the gate electrodes at 900.degree., in a H2O vapor atm, with a 8500 A **SiO2** cover, prior to the formation of the source and drain regions in the fabrication of insulated-gate field-effect **transistors**. **Wafers** of 1016 atoms/cm3 B-doped Si are coated with 1 .mu. perforated **SiO2**. Successive layers of 800 .ANG. **SiO2**, 250 .ANG. **SiN** and 1 .mu. 0.001 .OMEGA./cm p-type doped Si are deposited in the perforations. A gate electrode is made by photolithog. techniques. Then the **SiO2** seal is applied as indicated above. The **SiN** prevents oxidn. of the Si **wafer**. A final 1020 atoms/cm3 P doped **SiO2** is grown at 1100.degree. over the gate electrode and **wafer** so that some P diffuses into the border regions of the Si **wafer**, thus creating the source and drain regions of the **transistor**. The P-doped **SiO2** cover is removed with buffered HF. The **SiO2** protecting the p-type Si gate electrode is perforated and Al deposited to provide contacts for the gate electrode, the source and the drain.

L49 ANSWER 21 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1973:152946 HCAPLUS
DN 78:152946
TI Semiconductor components
IN Adam, Fritz Guenter; Obermeier, Cornelius; Renz, Albrecht; Gollinger, Wolfgang; Raabe, Martin
PA Deutsche ITT Industries G.m.b.H.
SO Ger. Offen., 16 pp.
CODEN: GWXXBX

12/04/2002

DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 2139631	A1	19730301	DE 1971-2139631	19710807
	DE 2139631	C3	19790510		
	IT 963314	A	19740110	IT 1972-27361	19720725
	AU 7245133	A1	19740207	AU 1972-45133	19720731
	GB 1339384	A	19731205	GB 1972-36232	19720803
	JP 48029370	A2	19730418	JP 1972-79014	19720807
PRAI	DE 1971-2139631		19710807		

AB In an insulated-gate, field-effect **transistor**, the distance between the edge of the polycryst. Si gate and the edge of the opening in the diffusion mask is kept to a controlled and reproducible min. Thus, a Si **wafer** is insulated first with **SiO_2**, then with Si_3N_4, both 400-2000 .ANG. thick. Next a polycryst. Si layer is applied, doped with B by planar diffusion, and the gate is developed by photomasking and etching. The edge of the gate is insulated by oxidn. in wet O. The drain and **source regions** are formed by planar diffusion.

12/04/2002

L50 ANSWER 1 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:833462 HCAPLUS
DN 137:331962
TI Method for forming ultra-shallow junctions using laser annealing in MOSFET **integrated circuits**
IN Sohn, Yong Sun
PA S. Korea
SO U.S. Pat. Appl. Publ., 14 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002160592	A1	20021031	US 2001-16534	20011210
	US 6475888	B1	20021105		
	JP 2002343734	A2	20021129	JP 2001-367836	20011130
PRAI	KR 2001-23403	A	20010430		

AB The invention relates to a process for making an ultra-shallow junction using laser annealing wherein an amorphous carbon layer is used as an energy absorber layer, the process comprising the steps of: prepg. a silicon substrate having isolation layers; forming a gate having a stacked structure of a gate insulating layer, a polysilicon layer and a metal **layer** on the **silicon** substrate; forming a sacrificial spacer on the sidewalls of the gate; forming **source** and **drain regions** on the silicon substrate regions at both sides of the gate including on the sacrificial spacer; removing the sacrificial spacer; doping impurities to form source/drain extension doping **layers** on the **silicon** substrate regions at both sides of the gate; depositing sequentially a reaction preventing layer and an amorphous carbon layer as a laser absorber layer on the resulting **structure**; forming **source**/drain extension doping layers on inner sides of the **source** and **drain regions** by performing laser annealing in an atm. of inert gas or under vacuum; and removing the amorphous carbon layer.

L50 ANSWER 2 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:716992 HCAPLUS
DN 137:240793
TI Method for fabricating a MOS **transistor** of an embedded memory
IN Chien, Sun-chieh; Kuo, Chien-li
PA Taiwan
SO U.S. Pat. Appl. Publ., 12 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002132429	A1	20020919	US 2001-798857	20010301
	US 6468838	B2	20021022		

AB The present invention provides a method for manufg. a MOS **transistor** of an embedded memory on the surface of semiconductor **wafer**. The method of present invention is 1st to define a memory array area and a periphery circuit region on the surface of the semiconductor **wafer** and to depose a dielec. layer, a undoped poly-**Si layer**, a silicide layer, a doped poly-**Si layer**, a protection layer and a photoresist layer sequentially. A plurality of gate patterns on the memory array area is

defined and the protection layer is etched to the surface of the doped poly-**Si layer**. A plurality of gate patterns on the periphery circuit region is defined in and the doped poly-**Si layer**, the silicide layer and the undoped poly-**Si layer** are etched to the surface of the dielec. layer so as to form gates of each MOS **transistors** in the memory array area and periphery circuit region. A spacer and **source** and **drain region** are formed around each gate.

L50 ANSWER 3 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:688544 HCAPLUS
DN 137:225243
TI Process flow to reduce spacer undercut phenomena
IN Wang, Ling-Sung; Chen, Ying-Lin
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6448167	B1	20020910	US 2001-27976	20011220

AB The invention relates to a process for making a composite insulator spacer on the sides of a MOSFET gate structure, wherein the underlying component of the composite insulator spacer is comprised of a thin **silicon** oxide **layer** obtained via chem. vapor deposition procedures using tetraethylorthosilicate (TEOS) as a source. To densify the underlying thin **silicon** oxide **layer** an anneal procedure usually performed after implantation of ions used for a lightly doped **source/drain region**, is delayed and performed after deposition of the thin **silicon** oxide **layer**. The anneal procedure is then used for both activation of the lightly doped source/drain ions, and densification of the thin **silicon** oxide **layer**. The etch rate of the densified **silicon** oxide **layer**, in dil. hydrofluoric acid procedures is now reduced allowing the underlying silicon oxide component, of the composite insulator spacer, to survive subsequent wet clean procedures employing dil. hydrofluoric acid.

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 4 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:627690 HCAPLUS
DN 137:148675
TI Method of manufacturing self-aligned silicide for embedded DRAM
IN Lin, Yung-Chang; Chen, Dung-Po; Chen, Shr-Yi
PA United Microelectronics Corp., Taiwan
SO Taiwan, 20 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 392222	B	20000601	TW 1998-87113484	19980817

AB The method comprises: sequentially forming a thin oxide **layer**, a **silicon nitride layer** and a thick oxide layer after annealing **source/drain region**; then, performing planarization process and etching process for precisely removing the isolation layer on the **source/drain**

region and gate of the **logic circuit** region, and on the gate of the memory cell region; afterwards, forming self-aligned silicide (salicide) on these regions. Therefore, the resistance values of these regions are decreased, and the operating speeds thereof are increased. Further, the **source/drain region** of the memory cell region is prevented from having silicide formed thereon, so as to avoid capacitor leakage. In addn., this step can be performed after annealing the **source/drain region**, such that thermal stability problem and inter-diffusion of polysilicon impurity in the gate oxide layer are prevented.

L50 ANSWER 5 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:612067 HCAPLUS
DN 137:162401
TI Manufacture of **integrated circuits** containing MISFETs
IN Mitani, Shinichiro; Ichinose, Katsuhiko; Saito, Tomohiro; Yanagida, Yohei
PA Hitachi Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002231938	A2	20020816	JP 2001-22133	20010130

AB The process includes: (a) forming gate insulator **films** on **Si** substrates, (b) forming elec. conductive films and patterning them into gate electrodes, (c) deposition of **Si** oxide **films** on the substrates as well as on the gate electrodes, (d) anisotropically etching the **Si** oxide **films** to form 1st sidewalls for the gate electrodes, (e) deposition of **Si nitride films** on the **Si** substrates, the 1st sidewall films and the gate electrodes, (f) anisotropically etching the **Si nitride films** to form 2nd sidewalls for the gate electrodes, (g) implanting impurities in the substrates with the 2nd sidewall films as masks to form **source/drain regions**, (h) cleaning the surface of the **source/ drain regions** with HF type solns., (i) deposition of metal films on the **source/drain regions**, (j) siliciding the metal films with the 2nd sidewall films as masks to form metal silicide layers at the contact **areas** of the **source /drain regions** and the metal films, and (k) removal of the nonreacting metal films. Current leaks in MISFETs are prevented, and fringe capacitance between the gate electrodes and the **source/ drain regions** is decreased.

L50 ANSWER 6 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:581865 HCAPLUS
DN 137:102402
TI Fabrication of short-channel nMOSFET having self-aligned silicide contact
IN Wu, Shie-Lin
PA TSMC-Acer Semiconductor Manufacturing Corporation, Taiwan
SO Taiwan, 20 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 399243	B	20000721	TW 1998-87102295	19980218

AB The invention grows an oxide **layer** on a **silicon**

substrate, then deposits a non-doped poly-crystal **silicon layer**. Next, a **silicon nitride** thin **layer** and an n+ doped poly-crystal **silicon layer** are deposited. This n+ doped poly-crystal **silicon layer** is back-etched to define the gate. A low-temp. oxygen vapor process oxidizes the n+ doped poly-crystal **silicon layer**. Using buffered oxide etchant (BOE) and dild. HF to remove the oxide film on the poly-crystal silicon gate; the residual doped poly-crystal silicon is used as the mask to etch **silicon nitride** coverage **layer**. Next, residual doped poly-crystal **silicon layer** and the **silicon nitride layer** coverage layer as the mask for etching non-doped poly-crystal **silicon layer** to form a short channel gate. Next, the phosphosilicate glass (PSG) sidewall spacer is formed. The **silicon nitride** coverage **layer** is removed. Next, a noble metal or refractory metal is deposited on all regions. High dose arsenic or phosphorus ions are implanted into the substrate to form the **source/drain region**. Next, two-step rapid thermal processing (RTP) process forms the self-aligned silicide contact to manuf. the short channel in nMOSFET.

L50 ANSWER 7 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:575698 HCAPLUS
DN 137:133266
TI Method for manufacturing semiconductor device on silicon-on-insulator substrate
IN Wu, Der-yuan; Liu, Chih-cheng
PA Taiwan
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002102813	A1	20020801	US 2001-774774	20010131

AB A method for manufg. a semiconductor device with a shallow channel on a silicon-on-insulator substrate is disclosed. The method uses a dielec. layer as a mask, an oxygen implantation and a heating process to form a **silicon dioxide layer** within a **silicon**-on-insulator substrate before forming a gate electrode on the silicon-on-insulator substrate. That is, the junction depth of the channel is reduced. First of all, a silicon-on-insulator substrate having a **silicon layer** and an insulating layer is provided, wherein the **silicon layer** is sepd. by the insulating layer. Secondly, a first dielec. layer is deposited on the **silicon layer**. Thirdly, a gate region pattern is transferred into the first dielec. layer to form a trench and expose the **silicon layer**. Then, oxygen mols. are implanted into the **silicon layer**, and the **silicon**-on-insulator substrate is heated to form a **silicon dioxide layer** therein. Next, a second dielec. layer is deposited and the trench is filled with the same. Then, two spacers are formed in the trench by anisotropically etching the second dielec. layer. Furthermore, a gate electrode is formed by filling the trench with a conductive layer. Moreover, the first dielec. layer is removed. Finally, **source** and **drain regions** are formed in the **silicon layer**.

L50 ANSWER 8 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:540210 HCAPLUS

DN 137:87119
TI **Transistor** structures.
IN Sandhu, Gurtej S.; Moore, John T.; Rueger, Neal R.
PA USA
SO U.S. Pat. Appl. Publ., 8 pp., Division of U.S. Ser. No. 633,556.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002094620	A1	20020718	US 2002-50348	20020115
	US 2002094621	A1	20020718	US 2002-50373	20020115
	US 2002098710	A1	20020725	US 2002-50347	20020115
PRAI	US 2000-633556	A3	20000807		

AB The invention encompasses a method of incorporating nitrogen into a **silicon**-oxide-contg. **layer**. The **silicon** -oxide-contg. **layer** is exposed to a nitrogen-contg. plasma to introduce nitrogen into the layer. The nitrogen is subsequently thermally annealed within the layer to bond at least some of the nitrogen to **silicon** within the **layer**. The invention also encompasses a method of forming a **transistor**. A gate oxide layer is formed over a semiconductive substrate. The gate oxide **layer** comprises **silicon dioxide**. The gate oxide layer is exposed to a nitrogen-contg. plasma to introduce nitrogen into the layer, and the layer is maintained at less than or equal to 400.degree. C. during the exposing. Subsequently, the nitrogen within the layer is thermally annealed to bond at least a majority of the nitrogen to silicon. At least one conductive layer is formed over the gate oxide layer. **Source/drain regions** are formed within the semiconductive substrate, and are gatedly connected to one another by the at least one conductive layer. The invention also encompasses **transistor** structures.

L50 ANSWER 9 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:447396 HCAPLUS
DN 137:14480
TI Manufacture of MISFETs
IN Koyama, Kazuhide
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002170958	A2	20020614	JP 2000-365541	20001130

AB The process includes: (a) forming device-isolating insulator layers on substrates in which thin **Si films** are formed on insulators, (b) forming gate insulator films and gate electrodes in the active regions defined by the device-isolating insulator layers, (c) 1st ion implantation of impurities in the active regions, (d) forming sidewalls to the gate electrodes, and (e) 2nd ion implantation of impurities where incident angle is set .gtoreq.7.degree.. Most suitable d. distribution is achieved in **source/drain regions**. Parasitic capacitance is decreased when thin SOI **wafers** are used.

L50 ANSWER 10 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:429492 HCAPLUS

12/04/2002

DN 137:26802
TI Fabrication method for a semiconductor **integrated circuit** device
IN Ono, Atsuki
PA Japan
SO U.S. Pat. Appl. Publ., 15 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002068405	A1	20020606	US 2001-988321	20011119
	JP 2002170887	A2	20020614	JP 2000-365447	20001130
PRAI	JP 2000-365447	A	20001130		

AB The present invention relates to a method of fabricating a semiconductor **integrated circuit** device in which p-channel MOS (Metal Oxide semiconductor) **transistors** (abbreviated as pMOS) having a gate insulation film composed of a **silicon** oxide-nitride **film** are mounted together with pMOS **transistors** having a gate insulation film composed of a **silicon** oxide **film** that is thicker than the **silicon** oxide-nitride **film**. The method fabricating a semiconductor **integrated circuit** involves a device in which 1st pMOS **transistors** having a gate insulation film composed of a **Si** oxide **film** are mounted together with 2nd pMOS **transistors** having a gate insulation film composed of a **Si** oxide-nitride **film** that is thinner than the **Si** oxide **film**; in which an impurity is implanted in advance in a polysilicon layer that is grown on the surfaces of the **Si** oxide **film** and the **Si** oxide-nitride **film** in only those positions at which 2nd pMOS **transistors** are to be formed before patterning the polysilicon layer into gate electrodes. The polysilicon layer is then patterned to form gate electrodes, following which the gate electrodes and Si substrate are each implanted with impurity to form **source-drain regions**.

L50 ANSWER 11 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:182224 HCAPLUS
DN 136:239972
TI **Transistor** and a method for forming the **transistor** with elevated and/or relatively shallow **source/drain regions** to achieve enhanced gate electrode formation in MOSFET
IN Gardner, Mark I.; Fulford, H. Jim; Kadosh, Daniel
PA Advanced Micro Devices, Inc., USA
SO U.S., 15 pp., Division of U.S. Ser. No. 78,828, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6355955	B1	20020312	US 2000-503979	20000214
PRAI	US 1998-78828	B3	19980514		

AB An **integrated circuit** fabrication process is provided for forming a **transistor** having shallow effective **source/drain regions** and/or laterally shortened **source/drain regions**. In 1 embodiment a mesa is formed from the semiconductor substrate. The mesa preferably extends from an upper surface of the semiconductor substrate. A gate conductor is preferably formed on a dielec. layer which is formed on an upper surface

of the mesa. LDD **areas** and **source/drain regions** are formed such that the regions are substantially contained within the mesa. In another embodiment, a gate conductor material is deposited within a trench, the trench being lined with a gate dielec. material, formed in a semiconductor substrate. The deposited gate conductor material is etched to form a gate conductor in which a lower surface of the gate conductor is substantially below an upper surface of the Si substrate. **Source/drain regions** are formed within the semiconductor substrate such that the effective depth of the formed **source/drain regions** is minimized.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 12 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:592225 HCAPLUS
DN 135:145768
TI Method for making high-aspect-ratio contacts on **integrated circuits** using a borderless pre-opened hard-mask technique
IN Huang, Jenn Ming
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6274471	B1	20010814	US 1999-325953	19990604

AB A method for fabricating high-aspect-ratio contacts on **integrated circuits**, such as embedded DRAMs, using a borderless pre-opened hard-mask technique is achieved. After forming gate electrodes for field effect **transistors** (FETs) and local interconnections from a polycide **layer** having a **Si nitride** (Si_3N_4) hard mask or cap layer, an anti-reflective coating was used to protect the FET **source/drain areas**. A photoresist mask and plasma etching were used to remove portions of the hard mask on the interconnections for contact openings, while the anti-reflective protects the **source/drain areas**. The photoresist mask and the anti-reflective coating are removed, and an interlevel dielec. (ILD) layer is deposited. The high-aspect-ratio contact openings can now be etched in the ILD layer to the **source/drain areas**, while concurrently etching reliable contact openings to the polycide interconnections where the cap Si_3N_4 was removed without overetching the **source/drain areas**.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 13 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:537445 HCAPLUS
DN 135:101075
TI MOS **transistor** with minimal overlap between gate and source/drain extensions
IN An, Judy Xilin; Yu, Bin; Liu, Yowjuang W.
PA Advanced Micro Devices, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO. KIND DATE APPLICATION NO. DATE

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6265256	B1	20010724	US 1998-156238	19980917

PI US 6265256 B1 20010724 US 1998-156238 19980917

AB A method for making a ULSI MOSFET includes establishing a gate void in a field oxide **layer** above a **Si** substrate, after **source** and **drain regions** with assocd. **source** and drain extensions have been established in the substrate. A gate electrode is deposited in the void and gate spacers are likewise deposited in the void on the sides of the gate electrode, such that the gate electrode is spaced from the walls of the void. The spacers, not the gate electrode, are located above the source/drain extensions, such that fringe coupling between the gate electrode and the source and drain extensions is suppressed.

RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 14 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:391997 HCAPLUS
DN 134:360344
TI Method for forming a **transistor** with reduced source/drain series resistance which enhances running speed and reduces operating temperature of **integrated circuits**
IN Hsu, Kirk; Lin, Yung-chang; Lin, Wen-jeng
PA United Microelectronics Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6238958	B1	20010529	US 1999-477109	19991231

AB A method for forming a **transistor** in **integrated circuits** is disclosed. The method includes the following steps. A substrate is 1st provided. An insulating layer is then formed on the substrate. A conductor layer is formed on the insulating layer. Subsequently, a patterned photoresist layer is formed on the conductor layer. Next, an etch process was used to etch the conductor layer which has a sidewall. The patterned photoresist layer is then removed. After forming a liner layer on the sidewall of the conductor layer, a lightly doped drain is formed on and in the substrate. Then, a spacer is formed on the liner layer. Thereafter, a proper process was used to introduce ions into the lightly doped drain, and then a **source/ drain region** is completed. The steps with follow include annealing the **source/drain region** and removing the spacer. Subsequently, an epi-**Si layer** is formed on the lightly doped **drain region**, the **source/drain region** and the top surface of the conductor layer. Finally, the epi-**Si layer** is treated with a salicidation process to form a salicide layer.

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 15 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:185271 HCAPLUS
DN 134:216022
TI Fabrication of a **transistor integrated circuit**
IN Samabedam, Skylance B.; Tobin, Phillip J.; Phillips, Anna M.; Dip, Anthony
PA Motorola, Inc., USA
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent

12/04/2002

LA   Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001068673	A2	20010316	JP 2000-216251	20000717
PRAI	US 1999-358614	A	19990721		

AB   The invention relates to process for making a semiconductor device, i.e., a **transistor integrated circuit**, wherein the liner layer and spacer layout of the elevated **source-drain region** minimizes the problem of facet formation in the epitaxial **Si film**.

L50 ANSWER 16 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN   2001:161460 HCAPLUS
DN   134:187136
TI   High density MOSFET fabrication method with integrated device scaling
IN   Gardner, Mark I.; Gilmer, Mark C.
PA   Advanced Micro Devices, Inc., USA
SO   U.S., 9 pp.
     CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6197644	B1	20010306	US 1998-187258	19981106

AB   In an **integrated circuit**, a pair of IGFET devices can be formed with reduced dimensions without requiring the use of higher resoln. optical masks. A gate electrode is formed with a **layer** of **Si nitride** and a photoresist layer formed thereon. The dimensions of the photoresist layer are reduced by a trim etch and the dimension of the nitride layer reduced by a nitride etch. After removing the photoresist **layer**, a **Si** oxide **layer** is grown over the exposed gate electrode and substrate. The nitride layer is removed leaving a pattern in the **Si** oxide **layer**. An anisotropic etch guided by the pattern in the **Si** oxide **layer** divides the gate electrode into two portions with an aperture there between. By proper doping, a IGFET structure can be formed that has two IGFET devices having a shared **source/drain region** and occupying the same area on the surface of the substrate as a single IGFET device previously occupied.
RE.CNT 10   THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
              ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 17 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN   2000:823305 HCAPLUS
DN   134:12397
TI   Fabrication of semiconductor **integrated circuit** and **integrated circuit** itself
IN   Ikeda, Yoshihiro; Tsuchiya, Osamu; Okazaki, Tsutomu
PA   Hitachi, Ltd., Japan
SO   Jpn. Kokai Tokkyo Koho, 8 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000323681	A2	20001124	JP 1999-133676	19990514

AB   A method for fabricating a semiconductor **integrated circuit** having a first group of MIS **transistors** with

gate electrodes spaced apart by a first spacing and a second group of MIS **transistors** with gate electrodes spaced apart by a second spacing involves forming a gate insulator film and gate electrodes on a semiconductor substrate, forming a pair of low-concn. semiconductor regions for comprising portions of **source/drain regions** of the first and second groups of MIS **transistors**, successively depositing first and second insulator films on the substrate, anisotropically etching to form a side wall spacer from the second insulator film on the gate electrodes covered with the first insulator film, forming a pair of high-concn. semiconductor regions for comprising the other portions of the **source/drain regions** of the first group, removing the second insulator film, and anisotropically etching to form a side wall spacer for the gate electrodes of the first and second groups from the first insulator film. Specifically, the second group of MIS **transistors** may comprise MISFET for memory cell selection, and the first and second insulator **films** may comprise **Si nitride** and **silica**, resp.

L50 ANSWER 18 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:547435 HCAPLUS
DN 133:128716
TI Method for forming electrostatic discharge (ESD) protection circuit for **integrated circuits**
IN Hsu, Chen-Chung
PA United Microelectronics Corp., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6100141	A	20000808	US 1998-186305	19981104

AB A method for forming a dual-thickness gate oxide layer starts with forming and patterning a pad oxide **layer** and a **Si nitride layer** on a substrate. The substrate contains pre-detd. regions for accommodating the internal circuit and the ESD protection circuit resp. A field oxide layer for sepg. the active regions of the internal circuit and the ESD protection circuit is formed by performing an oxidn. process. A thick gate oxide layer is formed on the active region of the ESD protection circuit by oxidn. after the pad oxide and the **Si nitride** there over are removed. Similarly, a thin gate oxide layer is formed on the active region of the internal circuit by oxidn. after the pad oxide and the **Si nitride** there over are removed. A patterned conducting layer is then formed on the substrate as gates. An implantation process was performed to form the **source/drain regions** within the region of the internal circuit. Next, spacers that surround the gates are formed on the substrate. And then, another implantation process was performed to form **source/drain regions** on the substrate within the region of the ESD protection circuit after the thick gate oxide layer is patterned to expose the substrate underneath.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 19 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:506093 HCAPLUS
DN 133:98144
TI Integrated circuitry and semiconductor processing method of forming field-effect **transistors**

12/04/2002

IN Trivedi, Jigish D.; Wang, Zhongze; Yang, Rongsheng
PA Micron Technology, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6093661	A	20000725	US 1999-386076	19990830
	US 2001040256	A1	20011115	US 1999-444024	19991119
	US 6417546	B2	20020709		
	US 2002079542	A1	20020627	US 2002-87416	20020227
PRAI	US 1999-386076	A3	19990830		
	US 1999-444024	A1	19991119		

AB In accordance with an aspect of the invention, a semiconductor processing method of forming field-effect **transistors** (FETs) includes forming a first gate dielec. layer over a first area configured for forming p-type FETs and a second area configured for forming n-type FETs, both areas on a semiconductor substrate. The first gate dielec. **layer** is **silicon dioxide** having a nitrogen concn. of 0.1% molar to 10.0% molar within the first gate dielec. layer, the nitrogen atoms being higher in concn. within the first gate dielec. layer at one elevational location as compared to another elevational location. The first gate dielec. layer is removed from over the second area while leaving the first gate dielec. layer over the first area, and a second gate dielec. layer is formed over the second area. The second gate dielec. **layer** is a **silicon dioxide** material substantially void of nitrogen atoms. **Transistor** gates are formed over the first and second gate dielec. layers, and then p-type **source/drain regions** are formed proximate the **transistor** gates in the first area and n-type **source/ drain regions** are formed proximate the **transistor** gates in the second area.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 20 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:464569 HCAPLUS
DN 133:67331
TI Method of forming self-aligned silicide MOSFET with an extended ultra-shallow source and drain junction
IN Wu, Shye-lin
PA Texas Instruments - Acer Incorporated, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6087234	A	20000711	US 1997-994178	19971219

AB The method includes forming a gate oxide layer on the substrate. A polysilicon layer is formed on the gate oxide layer. Then, a photog. and etching steps are used to form a gate structure. An oxidn. is performed on the substrate and the gate structure to form an first oxide layer on the substrate and on the surface of the polysilicon gate. A **silicon nitride layer** is deposited on the first oxide layer. A side-wall spacers is formed on the side walls of the gate structure, a first portion of the first oxide layer remaining between the gate structure and the side-wall spacers, and a second portion of the

first oxide layer remaining under the side-wall spacers. Next, a first ion implantation performed into the substrate to form first doped ions regions to serves as **source** and **drain region** of the **transistor**. Then, the side-wall spacers is removed, therefore remained the second portion of the first oxide layer covered by the side-wall spacers. Subsequently, a second ion implantation performed through the second portion of the first oxide layer to form second doped ion regions to serve as an extended **source** and **drain region** of the **transistor**. A rapid thermal annealing performed to form an extended source and drain junction and aligned to the region of the side-wall spacers being disposed.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 21 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:388534 HCAPLUS
DN 133:11780
TI Enhanced structure for salicide MOSFET and its fabrication
IN Wang, Pi-Shan; Weng, Chun-Wen; Hsu, Jung-Hsien
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6074922	A	20000613	US 1998-42366	19980313
	US 6218716	B1	20010417	US 2000-527607	20000317
PRAI	US 1998-42366	A3	19980313		

AB A method for increasing salicide thickness and effective polysilicon width at a narrow polysilicon line while reducing resistance and reducing source/drain bridging risk in the fabrication of a silicided polysilicon gate is described. A polysilicon layer is provided overlying a gate oxide layer on a semiconductor substrate. A dielec. **layer**, such as **Si** oxide, is deposited overlying the polysilicon layer. The **Si** oxide **layer**, polysilicon layer, and gate oxide layer are patterned to form a polysilicon gate electrode having a **Si** oxide **layer** on top of the gate electrode. Dielec. spacers, such as **Si nitride**, are formed on the sidewalls of the gate electrode and the **Si** oxide **layer**. In an alternative, Si spacers may be formed between the gate and the **Si nitride** spacers to increase the effective width of the polysilicon line. **Source** and **drain regions** assocd. with the gate electrode are formed within the semiconductor substrate. The **Si** oxide **layer** on top of gate electrode is removed whereby the **Si nitride** spacers extend above the gate electrode. A metal silicide is formed on the top surface of the gate electrode and over the **source** and **drain regions**. The dielec. spacers extending higher than the gate electrode prevent source/drain bridging during silicidation. This completes the formation of the salicided polysilicon gate electrode.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 22 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:808612 HCAPLUS
DN 132:43704
TI Manufacture of a MOSFET having LDD **source/drain regions**
IN Yeh, Wen-kuan; Chen, Coming; Chou, George

PA United Microelectronics Corp., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6004852	A	19991221	US 1997-864217	19970528
PRAI	US 1997-36967P	P	19970211		

AB An LDD **source/drain region** is manufd. adjacent to a gate electrode using a single ion implantation step. The method begins by providing a polysilicon gate electrode on a gate oxide over a substrate and then providing a thin layer of CVD oxide over the gate electrode and over the substrate. A thicker, 2nd layer of a material different from the 1st **Si** oxide **layer** is deposited over the device and is etched back to form sidewall spacer structures alongside and spaced slightly from the gate electrode. The spacer structures formed from the 2nd layer are then used as a mask to etch the oxide layer where it is exposed over the active regions of the substrate and then the spacer structures are removed. The portion of the oxide layer that remains over the top and sides of the gate electrode and over portions of the substrate adjacent to the gate electrode is then used as a mask for an ion implantation process. Implantation through the mask forms a more lightly doped and more shallowly doped region in the substrate beneath the mask and a more heavily doped and more deeply doped region in the portions of the **source/drain regions** that were not covered by the mask. Accordingly, implantation through the mask formed in this way forms a complete **source/drain region** having a lightly doped **drain structure** alongside the FET of the **integrated circuit**. Formation of LDD **source/drain regions** in this manner saves a no. of manufg. steps, resulting in reduced turnaround time and reduced costs.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 23 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:796079 HCAPLUS
DN 132:43680
TI MISFET nonvolatile memory **integrated circuit** and fabrication thereof
IN Shukuri, Shoji; Meguro, Satoshi; Kuroda, Kenichi
PA Hitachi, Ltd., Japan
SO PCT Int. Appl., 93 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9965083	A1	19991216	WO 1998-JP2588	19980612

W: CN, JP, KR, SG, US
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE

AB The invention relates to a MISFET constituting a nonvolatile memory, composed of a gate electrode formed on a gate insulating film, an n+ semiconductor **region** (**drain**) whose one end is extended below the gate electrode, an n+ semiconductor **region** (high concn. **source**) formed so as to be at an offset position relative to the gate electrode, and an n- semiconductor **region** (low

concn. **source**) whose one end is extended below the gate electrode, wherein the portion of the gate insulating film on the drain side is a **silicon** oxide **film**, and the portion of the gate insulating film on the source side is a three-layer insulating structure including a **silicon** oxide **film**, a **silicon nitride film** and a **silicon** oxide **film**.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 24 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:56351 HCAPLUS
DN 130:103821
TI Method of fabricating metal-oxide semiconductor (MOS) **transistors** with reduced level of degradation caused by hot carriers
IN Yeh, Wen-Kuan; Chen, Coming; Tsai, Meng-Jin; Chou, Jih-Wen
PA United Microelectrics Corp., Taiwan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5861329	A	19990119	US 1996-764254	19961212
PRAI	TW 1996-85112827		19961019		

AB A method of fabricating a metal-oxide semiconductor (MOS) **transistor** is provided. This method is devised particularly to reduce the level of degrdn. to the MOS **transistor** caused by hot carriers. In the fabrication process, a plasma treatment is applied to the **wafer** so as to cause the forming of a thin **layer** of **Si nitride** on the **wafer** which covers the gate and the lightly-doped diffusion (LDD) **regions** on the **source/drain regions** of the MOS **transistor**. This thin **layer** of **Si nitride** acts as a barrier which prevents hot carriers from crossing the gate dielec. layer, such that the degrdn. of the MOS **transistor** due to hot carriers crossing the gate dielec. layer can be greatly minimized.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 25 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:12262 HCAPLUS
DN 130:74818
TI Fabrication of a high-density **integrated circuit**
IN Gardner, Mark I.; Kadosh, Daniel; Hause, Fred N.
PA Advanced Micro Devices, Inc., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5851883	A	19981222	US 1997-844975	19970423
	US 6365943	B1	20020402	US 1998-157644	19980921
PRAI	US 1997-844975	A3	19970423		

AB A dielec. layer is formed on the upper surface of a semiconductor substrate which includes a **Si** base **layer**. Thereafter, an upper **Si layer** is formed on the upper surface of

the dielec. layer. The dielec. layer and the upper **Si layer** are then patterned to form 1st and 2nd Si-dielec. stacks on the upper surface of the base **Si layer**. The 1st and 2nd Si-dielec. stacks are laterally displaced on either side of a channel region of the Si substrate and each includes a proximal sidewall and a distal sidewall. The proximal sidewalls are approx. coincident with the resp. boundaries of the channel region. Thereafter, proximal and distal spacer structures are formed on the proximal and distal sidewalls, resp., of the 1st and 2nd Si-dielec. stacks. A gate dielec. layer is then formed on exposed portions of the **Si** base **layer** over the channel region. Portions of the 1st and 2nd Si-dielec. stacks located over resp. **source/drain regions** of the base **Si layer** are then selectively removed. Si is then deposited to fill 1st and 2nd voids created by the selected removal of the stacks. The Si deposition also fills a Si gate region above the gate dielec. over the channel region. Thereafter, an impurity distribution is introduced into the deposited Si. The deposited Si is then planarized to phys. isolate the Si within the gate region from the Si within the 1st and 2nd voids, giving a **transistor** including a Si gate structure and 1st and 2nd **source/drain structures**.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L50 ANSWER 26 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:250757 HCAPLUS
DN 128:303027
TI Amorphous silicon on insulator VLSI circuit structures
IN Burns, Stanley G.; Gruber, Carl; Shanks, Howard R.; Constant, Alan P.; Landin, Allen R.; Schmidt, David H.
PA Iowa State University Research Foundation, Inc., USA
SO U.S., 23 pp., Cont. of U.S. Ser. No. 319,752, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5742075	A	19980421	US 1996-751785	19961118
	US 6017794	A	20000125	US 1997-974782	19971120
PRAI	US 1994-319752		19941007		
	US 1996-751785		19961118		

AB A thin film **transistor** on insulator **integrated circuit** is made up of a no. of thin film **transistors** formed with small feature size and densely packed to allow interconnection as a complex circuit. An insulating substrate, preferably flexible, serves as the support layer for the **integrated circuit**. Control gate metalization is carried on the insulating substrate, a dielec. layer is deposited over the control gate, and an amorphous **Si layer** with doped **source** and **drain regions** is deposited on the dielec. layer. Trenches are formed to remove the amorphous Si material between **transistors** to allow highly dense circuit packing. An upper interconnect level which forms connections to the source, drain, and gate regions of the thin film **transistors** also interconnects the **transistors** to form more complex circuit structures. Due to the dense packing of the **transistors** allowed by the trench isolation, the interconnecting foils can be relatively short, increasing the speed of the circuit.

L50 ANSWER 27 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:704278 HCAPLUS
DN 126:12977

TI Fabrication of 0.15 .mu.m SOI p-MOSFETs using synchrotron radiation x-ray lithography
AU Choi, Sang Soo; Jeon, Young Jin; Lyu, Jong-Son; Yoo, Hyung Joun
CS Semiconductor Technology Division, Electronics and Telecommunications Research Institute, Taejon, 305-600, S. Korea
SO Proceedings of SPIE-The International Society for Optical Engineering (1996), 2778(Pt. 1, 17th Congress of the International Commission for Optics, 1996, Pt. 1), 15-16
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB 0.15 .mu.M SOI p-MOSFETs were fabricated by XRL (x-ray lithog.) for gate and contact layers patterning and optical lithog. for other layers. We prepd. x-ray mask blank with 2 .mu.m thick **silicon nitride film** as a membrane. The additive process was utilized for x-ray mask fabrication. We deposited 10 nm thick chromium layer and 20 nm thick gold layer over the membrane for the effective absorber electroplating. 400 Nm thick gold film was electroplated as an absorber after the patterning by electron-beam lithog. using resist PMMA. For the XRL process, Alladin storage ring of 800 MeV energy in Wisconsin University in U.S.A. and Karl Suss XRS 200 stepper were utilized. We used SAL 603 neg. resist (from Shipley Co.) and AZ-PF pos. resist (from Hoechst Co.) of 0.75 .mu.m thickness for the patterning of gate poly-Si and contact hole, resp. The gap distance between mask and **wafer** on the stepper was set at 40 .mu.m in automatic mode and the irradn. dose was 200 mJ/cm2. The alignment accuracy, **die** by **die**, was better than 150 nm. SOI p-channel MOSFETs were fabricated by a conventional CMOS process except two XRL steps for the gate and contact layers on SIMOX SOI substrates. 6.5 Nm gate oxide was thermally grown in dry O2 ambient at 900 .degree.C. The final surface silicon thickness was about 0.1 .mu.m, while the thickness of the **source/drain region** was 0.03 .mu.m thinner than that of the channel region. The breakdown voltage BVdss between the source and drain measured at VG = 0 V and Id = 10 nA was larger than 4 V. The lower Id,sat was caused mainly due to the high source/drain resistance resulted from the non-silicided thin **Si layers**. We also measured the interface trap d. Dit by using the charge pumping current method to confirm any damage at the Si/**SiO2** interface of the p-MOSFET on the normal bulk-Si substrate. Measured Dit was about 4 .times. 1010 eV-1-cm-2.

L50 ANSWER 28 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:577606 HCAPLUS
DN 125:210377
TI Manufacture of semiconductor device
IN Kakihara, Seiki
PA Nippon Kokan Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08181326	A2	19960712	JP 1994-336711	19941226

AB A process for making a semiconductor **IC** device, esp., a thin-film **transistor**, suited for use in SRAM, wherein the **source-drain regions** are formed in a poly-**Si layer** by ion-implantation and CVD.

12/04/2002

L50 ANSWER 29 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:362658 HCAPLUS
DN 122:176519
TI Manufacturing small MOS field-effect **transistors** having improved barrier layers to hot-electron injection
IN Ahmad, Aftab; Thakur, Randhir P. S.
PA Micron Semiconductor, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5382533	A	19950117	US 1993-79322	19930618

AB A process for suppressing hot electrons in sub-half-micron MOS devices is described, where a gate oxide and a gate electrode are formed on the surface of a Si substrate and **source** and **drain regions** are ion implanted into the Si substrate using the gate electrode as a mask. The process includes forming a layer of **SiO2** over the gate electrode and over the **source** and **drain regions** of the substrate, and then introducing a barrier-layer-forming element into the layer of **SiO2** to form a thin barrier region to hot electrons at the interface between the Si substrate and the **SiO2**. In a preferred embodiment, N is introduced into the **SiO2** by heating the **wafer** in a rapid thermal processor and in the presence of a N-contg. gas at an elevated temp. for a predetd. time. The N-contg. gas may be NF3, NH3, or N2O. In an alternative embodiment, F atoms are introduced into the Si substrate either as the sole barrier-**layer**-forming element (**silicon** fluoride) or prior to the formation of the thin **Si nitride** region. The F atoms form good strong Si-F bonds in the Si substrate and thereby further enhance the hot-electron suppression. In a 3rd embodiment, N and F are reacted in a rapid thermal processor to form a composite barrier layer of Si3N4 and Si fluoride.

L50 ANSWER 30 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:208799 HCAPLUS
DN 112:208799
TI Chemical nature of encapsulant-semiconductor interface after rapid thermal annealing for indium phosphide MISFETs
AU Biedenbender, M. D.; Kapoor, V. J.
CS Dep. Electr. Comput. Eng., Univ. Cincinnati, Cincinnati, OH, 45221-0030, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (1989), 1144(Int. Conf. Indium Phosphide Relat. Mater. Adv. Electron. Opt. Devices, 1st), 208-16
CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
AB The chem. nature of the encapsulant-InP interface before and after rapid thermal annealing (RTA) was investigated using XPS. RTA was investigated for ion implanted InP metal-insulator-semiconductor field-effect **transistor** (MISFET) fabrication. **Si nitride films** were used to encapsulate InP for RTA at 700 to 800.degree. for 10 to 60 in pure N2 or H2. The chem. nature of the encapsulant-InP interactions was examd. using a sequence of high-resoln. XPS at four depths through the interfacial region for the In 3d5/2, P 2p, N 1s, Si 2p, and O 1s peaks. The possible interfacial native oxides obsd. from the In 3d5/2 peak were In-O-H compds. such as In(OH)3, InO-OH, or InO2. No InPO4 was obsd. in the P 2p peak. The N 1s peak had a component consistent with

N-H or N-N bonding in which the area decreased by 42 to 100% after RTA. Changes in the width of the silicon oxy-nitride component of the Si 2p and O 1s peaks indicated changes in the compn. of the interfacial oxides after RTA. InP MISFET's were made on 2 in. semi-insulating **wafers** using a 150 keV, 4 .times. 1013 cm-2 Si implant for the **source** and **drain regions**. The implanted substrates were rapid thermal annealed at 700.degree. for 30 in N2 or H2. The MISFET's were fabricated with a P oxide/**Si dioxide** gate insulator which had a P oxide region at the insulator-InP interface. The gate insulator had a breakdown field of 2.5 .times. 106 V/cm and a resistivity of 1 .times. 1015 .OMEGA.-cm. The InP MISFET's had transconductance of 27 mS/mm, channel electron mobility of 1200 cm2V-1s-1, and drain current drift of 7%.

L50 ANSWER 31 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1987:469220 HCAPLUS
DN 107:69220
TI Method of making an MOS field-effect **transistor** in an **integrated circuit**
IN Hsu, Sheng T.
PA RCA Corp., USA
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4660276	A	19870428	US 1985-764551	19850812
	DE 3626598	C2	19950622	DE 1986-3626598	19860806
	JP 2615016	B2	19970528	JP 1986-189475	19860811
PRAI	US 1985-764551		19850812		

AB A method is described for making a MOS field effect **transistor** structure having W silicide contact surfaces for the gate and **source** and **drain regions**. Protective oxide is very precisely positioned so that a W layer is formed on only selected Si surfaces by selective deposition. Next, a layer of polysilicon is formed on the W layer. The resulting structure is treated in an O atm. to form the desired W silicide. A **Si nitride** cap can also be used to cover the gate portion during source and drain formation.

L50 ANSWER 32 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1981:40355 HCAPLUS
DN 94:40355
TI Semiconductor device
PA Nippon Electric Co., Ltd., Japan
SO Jpn. Tokkyo Koho, 4 pp.
CODEN: JAXXAD
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 55028553	B4	19800729	JP 1979-54805	19790507

AB The design and fabrication are claimed of an insulated-gate field-effect semiconductor device for **integrated circuits**. The diffusion in the channel stopper region, the diffusion in the **source** and **drain regions**, and the formation of **SiO2** on the channel stopper region are carried out using an insulator film other than **SiO2** (e.g., Al2O3 or Si3N4).

12/04/2002

L68 ANSWER 1 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-638076 [69] WPIX
DNN N2002-504113 DNC C2002-180263
TI Fabrication of an insulated gate MOS **transistor** having silicon on insulator **structure** involves forming **source**, **drain** and channel **regions** in a silicon layer isolated from substrate.
DC L03 U11 U12
IN MONFRAY, S; SKOTNIKI, T; VILLARET, A; SKOTNICKI, T
PA (ETFR) FRANCE TELECOM; (SGSA) STMICROELECTRONICS SA
CYC 2
PI FR 2821483 A1 20020830 (200269)* 16p
US 2002135020 A1 20020926 (200270)
ADT FR 2821483 A1 FR 2001-2745 20010228; US 2002135020 A1 US 2002-84255 20020227
PRAI FR 2001-2745 20010228
AB FR 2821483 A UPAB: 20021026

NOVELTY - Fabrication of the insulated gate MOS **transistor** involves providing source (S), drain (D) and channel (30) regions in a silicon layer (3) completely isolated vertically from a support substrate (1) by an insulating layer (21) and bordered laterally by a lateral shallow trench isolation (STI) region.

DETAILED DESCRIPTION - Fabrication of an insulated gate MOS **transistor** involves:

(a) selective epitaxial formation, on the surface of a substrate bordered by a lateral STI region, a stack comprising a SiGe layer and a Si layer (3);

(b) formation of a gate oxide layer (40) on the stack;

(c) formation of a gate region (5) applied on the gate oxide layer (40);

(d) complete selective etching of the SiGe layer so as to form a tunnel (20), the etching being performed from the edges of the STI region in the direction of the gate (5), and filling the tunnel with an insulating material so as to vertically isolate the **transistor** from the substrate.

The thickness of the Si layer (3) is of the order of tens of nanometers, e.g. 20 nanometers.

An INDEPENDENT CLAIM is given for an **integrated circuit** in which source (S), drain (D) and channel (30) regions are formed in a silicon layer (3) completely isolated from a support substrate (1) by an insulating layer (21), and laterally bordered by a lateral STI region.

USE - **Integrated circuit** fabrication, especially insulated gate MOS **transistors** having a silicon-on-insulator (SOI) structure.

ADVANTAGE - The process allows production of SOI **transistors** with very thin Si film and **buried dielectric** having perfectly controlled thicknesses.

DESCRIPTION OF DRAWING(S) - The drawing shows an insulated gate MOS **transistor** according to the invention.

Substrate 1
Silicon layer 3
Gate 5
Insulating spacers 6
Insulating layer 21
Channel 30
Gate oxide 40
Drain region D
Source region S
Transistor T

Dwg.5/5

L68 ANSWER 2 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-526458 [56] WPIX
DNN N2002-416626 DNC C2002-149038
TI **Integrated circuit chip** protecting inputs of semiconductor circuits, has pad, substrate, first-type dopant well, first-type dopant contact region, power supply node, ground node coupled, and indirect connection.
DC L03 U11 U12 U13
IN BRENNAN, C J; JACUNSKI, M D; KILLIAN, M A; TONTI, W R
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6399990 B1 20020604 (200256)* 11p
ADT US 6399990 B1 US 2000-531362 20000321
PRAI US 2000-531362 20000321
AB US 6399990 B UPAB: 20020903

NOVELTY - An **integrated circuit** (**IC**) **chip** comprises a pad to be protected from electrostatic discharge (ESD); a substrate; first-type dopant well formed in the substrate; first-type dopant contact region; power supply node for powering the **IC chip**; ground node coupled to the contact region; and indirect connection to the contact region.

DETAILED DESCRIPTION - An **IC chip** comprises (i) a pad to be protected from ESD; (ii) a substrate; (iii) a first-type dopant well formed in the substrate; (iv) a first-type dopant contact region in the well near a surface of the substrate; (v) a second-type dopant region in the well near the surface of the substrate and coupled to the pad to be protected; power supply(s) node for powering the **IC chip** ; (vi) a ground node coupled to the contact region; and indirect connection to the contact region comprising a resistor(s) or a N-type metal oxide semiconductor **transistor** (20).

USE - For protecting inputs of semiconductor circuits.

ADVANTAGE - The invention does not damage the circuits to be protected or the protection circuit itself.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of an **integrated circuit**.

N-type metal oxide semiconductor **transistor** 20

Dwg.1/11

L68 ANSWER 3 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-517281 [55] WPIX
DNN N2002-409236 DNC C2002-146384
TI **Integrated circuit** manufacture involves forming several gate structures on upper **wafer** corresponding to buried insulator structures of lower **wafer**.
DC L03 U11 U12
IN LIN, M; PRAMANICK, S; YU, B
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6380019 B1 20020430 (200255)* 7p
ADT US 6380019 B1 US 1998-187498 19981106
PRAI US 1998-187498 19981106
AB US 6380019 B UPAB: 20020829

NOVELTY - Buried insulator structures (142) are formed in silicon **wafer** (112) by LOCOS or trench process. Another **wafer** (114) is attached on top surface of the **wafer** (112). Several gate structures (130) are formed on the **wafer** (114) above insulator structures in the lower **wafer**. The thickness between the insulator and gate structures is less than 80 nm.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for

ultra-large scale circuit manufacturing method.
USE - For fabricating **integrated circuit** e.g. ULSI circuit with MOSFET and local insulator structure.
ADVANTAGE - **Transistor** possesses superior immunity to short channeling effect, and achieve near ideal threshold voltage swings, as the distance between the insulator and gate structures is less than 80 nm. The availability of silicon-on-**wafer** below **source** and **drain regions** allows significant body thickness for appropriate silicidation, thereby assuring low **drain** and **source region** series resistance.
DESCRIPTION OF DRAWING(S) - The figures show cross-sectional views of the portion of the **integrated circuit**.
silicon **wafers** 112,114
gate structure 130
buried insulated structure 142
6,10,11/11

L68 ANSWER 4 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-505510 [54] WPIX
DNC C2002-143716
TI Method for manufacturing vertical **transistor** using standard semiconductor process.
DC L03 U11 U12 U13
IN LEE, J U
PA (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 1
PI KR 2002005233 A 20020117 (200254)* 1p
ADT KR 2002005233 A KR 2000-37368 20000630
PRAI KR 2000-37368 20000630
AB KR2002005233 A UPAB: 20020823
NOVELTY - A method for manufacturing a vertical **transistor** using a standard semiconductor process is provided to manufacture a high-integrated dynamic random access memory(DRAM) device and a high-performance complementary metal-oxide-semiconductor(CMOS) field-effect-**transistor**(FET), by forming the vertical **transistor** on a double layer silicon **wafer**.
DETAILED DESCRIPTION - After a part of an upper silicon layer is etched by a photolithography method, an ion implantation process is performed to form a **source/drain region**(4). The upper silicon layer is removed to separate devices by a photolithography method. An interlayer dielectric(5) is formed, and is planarized by a chemical mechanical polishing(CMP) method. The planarized interlayer dielectric is dry- or wet-etched to be left by a predetermined thickness from an interface between the upper silicon layer and a **buried oxide** layer(2). A gate oxide layer(6) and a gate material(7) are consecutively formed, and the gate material is planarized by a CMP method. A predetermined thickness of the gate material is wet- or dry-etched, and an interlayer dielectric(8) is formed. The gate material and the interlayer dielectric are etched by a photolithography method. The interlayer dielectric is etched to form a **source/drain region**(9) by a photolithography method. Doped polycrystalline silicon is formed by an ion implantation method or epitaxial growth method. The **source/drain region** is formed by a photolithography method.
Dwg.0/10

L68 ANSWER 5 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-490537 [52] WPIX
DNN N2002-387774 DNC C2002-139331
TI **Integrated circuit** manufacture involves implanting **source/drain area** with dopant species to form

buried doped regions and etching shallow trench isolation apertures about the buried doped regions.
DC L03 U11 U12
IN CHEN, B A; HIRSCH, A; IYER, S K; ROVEDO, N; WANN, H; ZHANG, Y
PA (IBMC) IBM CORP; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 23
PI WO 2002047144 A2 20020613 (200252)* EN 13p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: CN JP KR
US 2002072206 A1 20020613 (200252)
US 6429091 B1 20020806 (200254)
ADT WO 2002047144 A2 WO 2001-US45195 20011129; US 2002072206 A1 US 2000-733324 20001208; US 6429091 B1 US 2000-733324 20001208
PRAI US 2000-733324 20001208
AB WO 200247144 A UPAB: 20020815
NOVELTY - An **integrated circuit** is manufactured by implanting a set of **source/drain area** in a substrate with a dopant species to form a set of buried doped regions. Shallow trench isolation (STI) apertures are etched about the buried doped regions to define **transistor** regions and expose a surface of the buried doped regions in walls of the STI apertures.

DETAILED DESCRIPTION - Manufacture of an **integrated circuit** involves: preparing a semiconductor substrate; implanting a set of **source/drain area** in the substrate with a dopant species to form a set of buried doped regions; etching shallow trench isolation (STI) apertures about the buried doped regions to define **transistor** regions and expose a surface of the buried doped regions in walls of the STI apertures; filling the STI apertures and the buried cavities conformally with an STI insulator; forming **transistors** having source and drains disposed above the buried cavities; and connecting the **transistors** to form the **integrated circuit**.

USE - For manufacturing **integrated circuit**.

ADVANTAGE - The implantation of the dopant species at a dose two orders of magnitude is required for oxygen implantation to obtain a desired thickness of the buried layer. The dopant used makes the etching easier and provides less damage to the **transistor** device layer.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of a portion of an **integrated circuit** in which a p-type substrate has a pad nitride/oxide layer.
Dwg.1/9

L68 ANSWER 6 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-488583 [52] WPIX
DNN N2002-386141 DNC C2002-138728
TI Fabrication of silicon-on-insulator devices involves forming **source/drain regions** of lightly doped **drain structure** with physical isolation spaces on boundaries between channel **region** and **source/drain regions**.
DC L03 U11 U12 U13
IN LEE, J U; LEE, J W
PA (HYNI-N) HYNIX SEMICONDUCTOR INC; (LEEJ-I) LEE J W
CYC 2
PI US 2002034841 A1 20020321 (200252)* 9p
KR 2002001419 A 20020109 (200252)
US 6461903 B2 20021008 (200269)
ADT US 2002034841 A1 US 2001-874293 20010606; KR 2002001419 A KR 2000-36132 20000628; US 6461903 B2 US 2001-874293 20010606
PRAI KR 2000-36132 20000628

12/04/2002

AB US2002034841 A UPAB: 20020815
NOVELTY - Silicon-on-insulator devices are fabricated by forming **source/drain regions** of lightly doped **drain structure** having physical isolation spaces on boundaries between the **source/drain regions** and a channel region in an active region of an exposed semiconductor layer.

DETAILED DESCRIPTION - Fabrication of silicon-on-insulator (SOI) devices includes preparing an SOI **wafer** having a stack structure of a base substrate (11), a **buried oxide** film (12) and a semiconductor layer (13). A field oxide film is formed on the semiconductor layer to define an active region. A gate (22) on the active region of the semiconductor layer is formed and has two side walls. A dummy spacer is formed on the gate and the two side walls. A polycrystalline silicon film is formed at a selected width on the two side walls of the gate including the dummy spacer to form a resultant structure. An insulating film is deposited on the resultant structure. The insulating film is polished using the dummy spacer as a polishing stop layer. The polycrystalline silicon film is removed to expose a part of the semiconductor layer. A hole exposing a part of the **buried oxide** is formed by dry etching the exposed part of the semiconductor layer. The **buried oxide** film exposed through the hole and an area adjacent the hole is etched using a wet etching process. A silicon epitaxial layer is grown from a midpoint of the semiconductor layer to a point higher than an upper surface of the semiconductor layer on a side of the part of the semiconductor layer exposed by the hole using a selective epitaxial growth process. A surface of the silicon epitaxial layer is etched to be equivalent to a height of the semiconductor layer. The dummy spacer and the insulating film are removed. **Source/drain regions** (30a-b) of lightly doped **drain structure** is form. They have a first physical isolation space on a first boundary between a **source region** and a channel region (30c); and a second physical isolation space on a secondary boundary between a **drain region** and the channel region in the active region of the exposed semiconductor layer.

USE - For fabricating silicon-on-insulator devices.

ADVANTAGE - The inventive method fabricates part depletion type SOI devices capable of preventing a floating body effect (e.g., kink phenomenon) and a parasitic bipolar **transistor**, thus ensuring a stable operation performance. Thus, the obtained SOI device has improved characteristic and reliability.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of a part depletion type SOI device.

base substrate 11
buried oxide film 12
semiconductor layer 13
gate 22
source/drain regions 30a-b
channel region 30c
Dwg.2H/2

L68 ANSWER 7 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-425519 [45] WPIX
DNN N2002-334620 DNC C2002-120440
TI Formation of field-effect **transistor** in **integrated circuit** involves exposing buried insulating layer by removing portions of substrate using first sidewall spacers as masking material for defining active region.
DC L03 U11 U12 U13
IN HORSTMANN, M; RAAB, M; STEPHAN, R; WIECZOREK, K

PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 2
PI US 2002048862 A1 20020425 (200245)* 10p
DE 10052131 A1 20020508 (200245)
ADT US 2002048862 A1 US 2001-810771 20010316; DE 10052131 A1 DE 2000-10052131 20001020
PRAI DE 2000-10052131 20001020
AB US2002048862 A UPAB: 20020717
NOVELTY - A field-effect **transistor** is made by forming gate electrode over semiconductor substrate surface, forming first sidewall spacers along gate electrode sidewalls, and removing portions of substrate above a buried insulating layer and adjacent first sidewall spacer to expose the buried insulating layer. The first sidewall spacers are used as masking material for defining an active region.

USE - For forming a field-effect **transistor** in an **integrated circuit**.

ADVANTAGE - The inventive method does not include realigning steps yet producing a field-effect **transistor** that is precisely aligned to gate electrode within the active region. It requires less photolithography masks as compared to conventional processing. It produces field-effect **transistor** having increased circuit-density and decreased parasitic capacitances.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic cross-sectional view of a semiconductor substrate after sidewall spacer had been removed.

buried insulating layer 102
gate cover layer 103
gate electrode 104
active region 110

Dwg.2d/2

L68 ANSWER 8 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-370714 [40] WPIX
DNN N2002-289592
TI Insulated gate field-effect **transistor** using silicon on insulator substrate with N-type silicon layer to improve on-breakdown of **transistor** without size increase.
DC U11 U12
IN OHYANAGI, T; WATANABE, A
PA (HITA) HITACHI LTD
CYC 2
PI US 2001038125 A1 20011108 (200240)* 35p
JP 2001308338 A 20011102 (200240) 15p
ADT US 2001038125 A1 US 2001-829582 20010409; JP 2001308338 A JP 2000-131509 20000426
PRAI JP 2000-131509 20000426
AB US2001038125 A UPAB: 20020626
NOVELTY - An N-type channel lateral metal-oxide-semiconductor field-effect **transistor** (MOSFET) includes the drain electrode (16) contacting a high concentration N-type diffusion layer (62), also in contact with the N-type region (51) formed together with the other N-type regions (52,53) of the P-type lateral MOSFET, while a source electrode (107) is provided near to the trench. The P-type **source regions** (41,42) and N-type regions (52,53) are made to contact the **buried oxide** film (21) in order to suppress the influence from the displacement current.

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for a semiconductor **integrated circuit**.

USE - Manufacturing insulated gate field-effect **transistor**.

ADVANTAGE - Improved on-breakdown of **transistor** without size increase.

DESCRIPTION OF DRAWING(S) - The drawing shows part of an
integrated circuit
Drain electrode 16
Diffusion layer 62
N-type regions 51-53
Buried oxide layer 21
Dwg.10/18

L68 ANSWER 9 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-327602 [36] WPIX
CR 2000-194656 [17]; 2002-215610 [27]; 2002-291488 [33]; 2002-328865 [36]; 2002-360271 [39]; 2002-443190 [47]; 2002-470633 [50]; 2002-517811 [55]; 2002-546404 [58]
DNN N2002-256887
TI Field effect **transistor** manufacturing method, involves forming masking layer having opening over substrate, through which n-type and p-type dopants are added to substrate.
DC U11 U12 U13
IN HATAB, P; WU, Z
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6335246 B1 20020101 (200236)* 12p
ADT US 6335246 B1 Div ex US 1997-968085 19971112, US 2000-494836 20000131
FDT US 6335246 B1 Div ex US 6025232
PRAI US 1997-968085 19971112; US 2000-494836 20000131
AB US 6335246 B UPAB: 20020916
NOVELTY - A masking layer (28) is formed over a n-type substrate (22) and an opening having sidewalls (32,34) is etched on the layer. A n-type dopant and p-type dopant are added by halo-doping through the opening into the substrate. The sidewall spacers (44,46) are formed over the respective sidewalls. A **transistor** gate is formed within the opening, over the channel **region** and **source/drain regions** are formed near the channel region.
USE - For complementary metal **oxide** semiconductor (CMOS), **buried** channel PMOS **transistors** fabrication.
ADVANTAGE - Operating speed of the **transistors** is increased by providing lower source/drain junction capacitances. Lightly doped **drain** (LDD) **regions** and punch through implants are obtained reliably for buried channel PMOS **transistors**.
DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of semiconductor **wafer** fragment.
n-type semiconductor substrate 22
Masking layer 28
Sidewalls 32,34
Sidewall spacers 44,46
Dwg.7/15

L68 ANSWER 10 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-253722 [30] WPIX
CR 1997-076279 [07]; 1998-387041 [33]; 1999-287073 [27]
DNN N2002-195828 DNC C2002-075859
TI Formation of field effect **transistor** for metal oxide semiconductors, involves providing gate on semiconductor substrate, forming polysilicon layer, and providing dopant masking cap on the gate.
DC L03 U11 U12
IN WU, J Z; YOGANATHAN, S
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6309935 B1 20011030 (200230)* 16p
ADT US 6309935 B1 Div ex US 1995-440222 19950512, Cont of US 1996-695407 19960812, US 1998-89841 19980603

FDT US 6309935 B1 Div ex US 5571733, Cont of US 5773358
PRAI US 1995-440222 19950512; US 1996-695407 19960812; US 1998-89841 19980603
AB US 6309935 B UPAB: 20020513
NOVELTY - A field effect **transistor** is formed by providing a gate (25) on a semiconductor substrate (12); forming a polysilicon layer (30) on the substrate, defining a pair of extending polysilicon projections (32, 34); and providing a dopant masking cap on the gate, while doping the polysilicon projections with an n-type or a p-type conductivity enhancing dopant impurity.
USE - The method is used for forming a field effect **transistor** used in metal oxide semiconductors.
ADVANTAGE - The method provides a single polysilicon deposition, and a single CMP step for NMOS or PMOS. It enables production of shallow **source/drain** diffusion **regions** within the bulk substrate. It also eliminates metal to bulk silicon contacts for diffusion regions, and improves packing density without necessitating an n- and p-type surround of contacts. The polysilicon deposition is performed at faster rate.
DESCRIPTION OF DRAWING(S) - The figure is a perspective view of a semiconductor **wafer** fragment, i.e. field effect **transistor**.
Substrate 12
Gate 25
Polysilicon layer 30
Polysilicon projections 32, 34
Polysilicon region 19
Capping layer 44
Diffusion regions 50, 52
Dwg.8/10

L68 ANSWER 11 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-250939 [30] WPIX
DNC C2002-075205
TI Silicon-on-insulator device and manufacturing method thereof.
DC L03 U13
IN LEE, W C
PA (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 1
PI KR 2001045399 A 20010605 (200230)* 1p
ADT KR 2001045399 A KR 1999-48670 19991104
PRAI KR 1999-48670 19991104
AB KR2001045399 A UPAB: 20020513
NOVELTY - A method for manufacturing a silicon-on-insulator (SOI) device is to provide the same electrostatic discharge(ESD) protection circuit as a bulk device, by forming the ESD protection circuit of a bipolar **transistor** structure or bilateral diode switch structure, wherein composition elements are formed in the first silicon layer and a **buried oxide** layer.
DETAILED DESCRIPTION - A silicon-on-insulator (SOI) **wafer** having a **buried oxide** layer is interposed between the first silicon layer as a supporting unit and the second silicon layer supplying a device formation region. An etch blocking layer is formed on the SOI **wafer**. The etch blocking layer is patterned to be left only in the device formation region. The second silicon layer is etched to confine the device formation region by using the etch blocking layer as a mask. The first and second regions in a portion of the exposed **buried oxide** layer to confine emitter and collector regions of a bipolar **transistor**. A silicon epi layer having the same height as the **buried oxide** layer is grown in the first and second regions where the **buried oxide** layer

is eliminated. Impurity ions are implanted into the first silicon layer portion under the silicon epi layer to form a base of the bipolar **transistor**. A gate is formed in the device formation region. Impurity ions are implanted into the device formation region at both sides of the gate and the silicon epi layer to form a **source/ drain region** of a metal-oxide-semiconductor (MOS) **transistor** and an emitter/a collector of the bipolar **transistor**.

USE - None given.

Dwg.0/10

L68 ANSWER 12 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-205019 [26] WPIX
DNN N2002-156014 DNC C2002-062832
TI Fabrication of silicon-on-insulator metal oxide silicon field effect **transistor** by forming channel at recess channel region by etching, dummy spacers at etched film, and lightly doped **drain** and ion **regions**.
DC L03 U11 U12
IN OH, J H
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD; (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 3
PI US 2002009859 A1 20020124 (200226)* 10p
JP 2002033490 A 20020131 (200226) 8p
KR 2002003028 A 20020110 (200247)
US 6429055 B2 20020806 (200254)
ADT US 2002009859 A1 US 2001-891193 20010626; JP 2002033490 A JP 2001-170062 20010605; KR 2002003028 A KR 2000-37414 20000630; US 6429055 B2 US 2001-891193 20010626
PRAI KR 2000-37414 20000630
AB US2002009859 A UPAB: 20020424

NOVELTY - Silicon-on-insulator metal oxide-silicon field effect **transistor** is fabricated by forming a channel at a recess channel region by etching silicon film. Dummy spacers are formed at sidewalls of the etched active silicon film. Lightly doped regions are formed by implanting ions in the portions of the recess channel regions. Lightly doped ions regions are formed by removing the dummy spacers.

DETAILED DESCRIPTION - Fabrication of a silicon-on-insulator (SOI) metal oxide silicon field effect **transistor** (MOSFET) involves forming:

(a) a **buried oxide** film (11) and an active silicon film on SOI substrate (10);

(b) a first photoresist film on the active silicon film;

(c) a recess channel region by implantation of ions in a portion of the active silicon film exposed after the formation of the first photoresist film;

(d) a channel at the recess region by etching the active silicon film to a predetermined depth while using the first photoresist film as a mask;

(e) dummy spacers at opposite side walls of the etched active silicon film;

(f) a second photoresist film on a portion of the active silicon film exposed after the removal of the first photoresist film and on a gate (16);

(g) lightly doped **drain regions** by implantation of ions in the portion of the recess channel region;

(h) lightly doped ion regions (18) by removing the dummy spacers;

(i) spacers at opposite side walls of the recess channel region; and

(j) source and drain electrodes and a gate electrode on a structure obtained after the formation of **source** and **drain regions** (20, 21).

The second photoresist film is not formed on regions where the dummy

spacers are formed. Each lightly doped **drain region** is defined between the gate and one of the dummy spacers. Low-concentration impurity ions are implanted in portions of the recess channel region defined at opposite sides of the gate. High-concentration impurity ions are implanted in the active silicon film to form the **source** and **drain regions**.

USE - For fabricating SOI MOSFET.

ADVANTAGE - The inventive method is capable of improving variations in threshold voltage and a parasitic bipolar effect generated in the formation of fully depleted SOI semiconductor **integrated circuits**. It enables the manufacture of large-scale integration in systems using SOI devices or memories using known large-scale integration.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view illustrating an SOI MOSFET fabrication.

SOI substrate 10
Buried oxide film 11
Gate 16
Lightly doped ion regions 18
Source and **drain regions** 20, 21
Silicide film 22
Dwg.3/3

L68 ANSWER 13 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-204956 [26] WPIX
DNN N2002-155952 DNC C2002-062802
TI Semiconductor memory **integrated circuit** has bottom layer of floating gates of memory cells and gate electrodes of peripheral circuit self-aligned with device isolation insulating film formed before burying the film.
DC L03 U11 U13
IN MORI, S
PA (TOKE) TOSHIBA KK
CYC 2
PI US 2002008278 A1 20020124 (200226)* 53p
JP 2002064157 A 20020228 (200231) 25p
ADT US 2002008278 A1 US 2001-876019 20010608; JP 2002064157 A JP 2001-171612 20010606
PRAI JP 2001-171612 20010606; JP 2000-174127 20000609
AB US2002008278 A UPAB: 20020424

NOVELTY - A semiconductor memory **integrated circuit** has at least the bottom layer of floating gates of nonvolatile memory cells and at least the bottom layer of gate electrodes of **transistors** in peripheral circuit formed before device isolation insulating film is buried, and maintained in self-alignment with the device isolation insulating film.

DETAILED DESCRIPTION - A semiconductor memory **integrated circuit** comprises: a semiconductor substrate; a device isolation insulating film buried in grooves formed into the substrate; a cell array having an arrangement of electrically erasable and programmable nonvolatile memory cells made by stacking floating gates and control gates on the semiconductor substrate; and a peripheral circuit disposed around the cell array on the substrate. At least the bottom layer of the floating gates of the nonvolatile memory cells and at least the bottom layer of gate electrodes of **transistors** in the peripheral circuit are formed before the device isolation insulating film is buried, and maintained in self-alignment with the device isolation insulating film. Impurities are doped into memory cell region and peripheral circuit region under different conditions from each other.

An INDEPENDENT CLAIM is also included for a method of manufacturing a semiconductor memory **integrated circuit** comprising:
forming gate insulating films for a cell array region and a peripheral

circuit region on a semiconductor substrate (10); forming a first-layer gate electrode material film (22) not doped with impurities on the gate insulating films; etching the substrate covered with the first-layer gate electrode material film to make grooves for device isolation and burying the device isolation grooves (13) with a device isolation insulating film (14); forming a second-layer gate electrode material film (24) not doped with impurities on the first-layer gate electrode material film maintained in self-alignment with regions surrounded by the device isolation insulating film and on the device isolation insulating film; selectively introducing impurities into the first-layer and second-layer gate electrode material films in the cell array region; selectively etching the second-layer gate electrode material film to isolate it on the device isolation insulating film in the cell array region; forming a gate insulating film (26) on the second-layer gate electrode material film to serve as an insulation film between floating gates and control gates of memory cells; removing the gate insulating film from the peripheral circuit region; forming a third-layer gate electrode material film (28) not doped with impurities on the gate insulating film; processing the gate electrode material in the memory cell region and the peripheral circuit region into a desired pattern to form control gate and floating gates in the memory cell region and form gate electrodes (G11, G12, G21, G22) in the peripheral circuit **region**; and forming **source** and drain diffusion layers and lowering the resistance of the gate electrodes by introducing impurities into the memory cell region and peripheral circuit region under different conditions.

USE - None given.

ADVANTAGE - The invention ensures impurity doping individually optimum for floating gates and control gates of memory cells, and gate electrodes of the peripheral circuit. At least the bottom layer of gate electrodes in the cell array region and the peripheral circuit region is stacked before the device isolation insulating film is buried. This bottom layer remains in self-alignment with the device isolation insulating film. The device isolation insulating film in the peripheral circuit region is prevented from retraction. Property and reliability of the peripheral circuit **transistors** can be improved.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a step of making a tunnel insulating film of flash memory.

Substrate 10
Device isolation grooves 13
Device isolation insulating film 14
First-layer gate electrode material film 22
Second-layer gate electrode material film 24
Gate insulating film 26
Third-layer gate electrode material film 28
Gate electrodes G11, G12, G21, G22

Dwg.14C/36

L68 ANSWER 14 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-132094 [18] WPIX
DNN N2002-099645 DNC C2002-040655
TI Lateral metal-oxide semiconductor field effect **transistor** as switch in power converter train, includes silicon carbide layer, gate, and **source** and **drain regions**.
DC L03 U11 U13 U21
IN LOTFI, A W; TAN, J; LOFTI, A W
PA (LUCE) LUCENT TECHNOLOGIES INC
CYC 30
PI EP 1104028 A2 20010530 (200218)* EN 12p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
BR 2000006785 A 20010904 (200218)

CN 1297258 A 20010530 (200218)
JP 2001196584 A 20010719 (200218) 11p
KR 2001051900 A 20010625 (200218)
ADT EP 1104028 A2 EP 2000-310082 20001113; BR 2000006785 A BR 2000-6785 20001113; CN 1297258 A CN 2000-130957 20001122; JP 2001196584 A JP 2000-355235 20001122; KR 2001051900 A KR 2000-70032 20001123
PRAI US 1999-448856 19991123
AB EP 1104028 A UPAB: 20020319
NOVELTY - A lateral metal-oxide semiconductor field effect **transistor** (MOSFET) (107) consists of a silicon carbide layer (110) in a substrate of a semiconductor **wafer**, a gate (121) on the silicon carbide layer, and source (125) and **drain** (130) **regions** which are located in the silicon carbide layer and laterally off-set from the gate.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for (A) a method of forming a lateral MOSFET on a substrate of a semiconductor **wafer**; (B) power converter comprising an isolation transformer, primary and secondary side power switches, where one of the power switches is a MOSFET, a drive circuit having a complementary metal oxide semiconductor (CMOS), an output inductor, and an output capacitor; and (C) method of forming a power converter.

USE - As a switch in a power converter train (claimed).

ADVANTAGE - The MOSFET exhibits a high breakdown voltage and a low on-resistance as a switch.

DESCRIPTION OF DRAWING(S) - The figure shows a semiconductor **wafer** having the inventive MOSFET.

Lateral MOSFET 107
Silicon carbide layer 110
Gate 121
Source region 125
Drain region 130
Dwg.1/4

L68 ANSWER 15 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-074273 [10] WPIX
DNN N2002-054763 DNC C2002-021973
TI Manufacture of semiconductor **structures** involves growing **source**/drains that are thicker in regions of larger gate-to-gate pitch, and doping source/drains with dopant(s) so that dopants abut underlying insulator layer.
DC L03 U11 U13
IN MOCUTA, A C; PARK, H; RAUSCH, W
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 2
PI US 6303450 B1 20011016 (200210)* 6p
CN 1354505 A 20020619 (200263)
ADT US 6303450 B1 US 2000-717971 20001121; CN 1354505 A CN 2001-130375 20011121
PRAI US 2000-717971 20001121
AB US 6303450 B UPAB: 20020213
NOVELTY - Semiconductor structures are made by providing a silicon **wafer** with an underlying insulator layer, providing gates adjacent to **source/drain regions**, growing **source/drains** between the gates so that source/drains are thicker in regions of larger gate-to-gate pitch, and doping the source/drains with dopant(s) so that the dopants abut the underlying insulator layer.

USE - For making semiconductor structures, particularly complementary metal oxide semiconductor structures, e.g. metal oxide semiconductor field effect **transistors**.

ADVANTAGE - The method makes semiconductor structures at deep

submicron scale that exhibit reduced canyon effects, facet effects, and lateral dopant diffusion.
DESCRIPTION OF DRAWING(S) - The figure shows a step of the process.
Buried oxide layer 2
Dopants 10
Dwg.8/8

L68 ANSWER 16 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2001-578509 [65] WPIX
DNN N2001-430425
TI Parasitic capacitance reducing method for use during fabrication of **integrated circuit**, involves forming air-gaps between gate and **dielectric** layer by **encapsulating** holes.
DC U11
IN LEE, C
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 6238987 B1 20010529 (200165)* 6p
ADT US 6238987 B1 US 1999-394636 19990913
PRAI US 1999-394636 19990913
AB US 6238987 B UPAB: 20011108
NOVELTY - Spacers are formed on both sides of gate (104) formed on gate oxide layer (102) of substrate (100). A chemical-mechanical polishing of surface of dielectric layer (114) is performed such that dielectric layer is lower than spacer top. Holes are formed between gate and dielectric layer by removing spacers. Then, holes are encapsulated to form air-gaps (120).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for air-gap forming method.
USE - For reducing parasitic capacitance during fabrication of **integrated circuit** such as metal oxide semiconductor field effect **transistor** (MOSFET).
ADVANTAGE - By forming air-gaps parasitic capacitance between **transistor** gate and **source/drain region** is reduced, as a result, RC time delay is reduced and operating speed is improved.
DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view to explain parasitic capacitance reducing method.
Substrate 100
Gate oxide layer 102
Gate 104
Dielectric layer 114
Air-gaps 120
Dwg.1D/1

L68 ANSWER 17 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2001-396491 [42] WPIX
DNN N2001-292045
TI Silicon on insulator field effect **transistor** has narrow conductive perforation in **buried oxide** layer for electrically coupling channel region to semiconductor substrate.
DC U11 U12
IN JU, D
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6229187 B1 20010508 (200142)* 7p
ADT US 6229187 B1 US 1999-420972 19991020
PRAI US 1999-420972 19991020
AB US 6229187 B UPAB: 20010726
NOVELTY - Active region has central channel (26) sandwiched by source (28) and drain (30). A portion of active region (48) is isolated from substrate

by insulating oxide layer. An insulating trench (32) isolates the active region from other structures on substrate. The channel region is coupled to substrate by a conductive perforation (36) that is narrower than central channel **region** from **source** to **drain region**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a semiconductor device.

USE - Used in **transistor** fabrication.

ADVANTAGE - Decreases the power consumption by providing low function capacitance and low off state leakage. Reduces the size by providing small surface area for electrical isolation of various **transistors**. Eliminates floating body effect by fabricating unoxidized perforation on **wafer**.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of FET form an silicon substrate with perforated **buried oxide** layer.

Active region 18
Buried oxide layer 20
Channel 26
Source 28
Drain 30
Insulating trench 32
Perforation 36
Dwg.1/8

L68 ANSWER 18 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2001-334542 [35] WPIX
DNN N2001-241390
TI Silicon-on-insulator **logic circuit** for static RAM (SRAM) has field effect **transistor** (FET) with source potential lowered to charge pump potential at wait portion of clock signal maintaining channel at preset potential.
DC U12 U13
IN WOLLESEN, D L
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6201761 B1 20010313 (200135)* 9p
ADT US 6201761 B1 US 2000-491823 20000126
PRAI US 2000-491823 20000126
AB US 6201761 B UPAB: 20010625

NOVELTY - Charge pump voltage signal with a negative voltage pulse occurring at wait portion of a clock signal (68) is coupled to **source region** (52) of the N-channel FET (40) by switch (72). Source potential is lowered to the charge pump potential during negative voltage pulse period to create a forward bias junction between source and P-type channel (58) dropping the potential in channel region to preset value.

DETAILED DESCRIPTION - The circuit consists of a silicon-on-insulator substrate (48) separated from a silicon device layer (42) by an insulating **buried oxide** layer (46). The field effect **transistor** formed on the silicon device layer has **source region** (52) and **drain region** (54) of specific semiconductor conductivity, and a gate electrode (56) defining an electrically isolated central channel region of the opposite semiconductor conductivity between **source** and **drain regions**. A clock signal controlling the operation of the switch has a clock period with an active portion and a wait portion.

INDEPENDENT CLAIMS are also included for the following:

(a) floating body potential control; and

(b) static random access memory cell.

USE - Static random access memory.

ADVANTAGE - The maintenance of the channel region potential of the FET at preset voltage ensures that FET threshold voltage remains controlled so improving control of operating speed and access time of the memory cell.

DESCRIPTION OF DRAWING(S) - The figure shows cross-section of silicon on insulator field effect **transistor**.

N-channel FET 40
Silicon device layer 42
Buried oxide layer 46
Silicon-on-insulator substrate 48
Source region 52
Drain region 54
Gate electrode 56
P-type channel region 58
Clock signal 68
Switch 72
Dwg.2/8

L68 ANSWER 19 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2001-299514 [31] WPIX
DNN N2001-214823
TI Field effect **transistor** for motor vehicle, has silicon carbide layer and insulating layer which encapsulates active source, **drain** and channel **region**, formed on substrate.
DC U11 U12
IN HARRIS, C; KONSTANTINOV, A; SAVAGE, S
PA (ACRE-N) ACREO AB
CYC 92
PI WO 2000065660 A2 20001102 (200131)* EN 20p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2000046347 A 20001110 (200131)
US 6278133 B1 20010821 (200150)#
EP 1186053 A2 20020313 (200225) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
KR 2002002436 A 20020109 (200246)
CN 1347570 A 20020501 (200252)
ADT WO 2000065660 A2 WO 2000-SE773 20000420; AU 2000046347 A AU 2000-46347 20000420; US 6278133 B1 US 1999-298116 19990423; EP 1186053 A2 EP 2000-928059 20000420, WO 2000-SE773 20000420; KR 2002002436 A WO 2000-SE773 20000420, KR 2001-713472 20011022; CN 1347570 A CN 2000-806545 20000420
FDT AU 2000046347 A Based on WO 200065660; EP 1186053 A2 Based on WO 200065660; KR 2002002436 A Based on WO 200065660
PRAI SE 1999-1440 19990422; US 1999-298116 19990423
AB WO 200065660 A UPAB: 20010607
NOVELTY - **Source-drain regions** (4,5) separated by channel layer (6) are formed on substrate. Low doped silicon carbide layer (7) with doping concentration below 1016cm-3 and catalytic metal gate electrode (12) are formed on source, **drain** and channel **regions**. Insulating layer (13) with doping concentration below 2 multiply 1015 10-3 formed on layer (7), separate gate electrodes from source, **drain** and channel **regions**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **transistor** manufacturing method.

USE - Used as gas sensor in **IC** engine of motor vehicle.

ADVANTAGE - Provision of insulating layers on active source, **drain** and channel **regions**, encapsulates and protects them from atmosphere, thus **transistor** performs stable operation at high temperature upto 800 deg. C. Improves temperature stability and sensitivity of **transistor**.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of field effect **transistor**.

Source region 4
Drain region 5
Channel layer 6
Low doped silicon carbide layer 7
Gate electrode 12
Insulating layer 13
Dwg.1/5

L68 ANSWER 20 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2001-079489 [09] WPIX
DNN N2001-060486 DNC C2001-022738
TI Fabrication of semiconductor device for use as, e.g. **integrated circuit**, comprises defining prospective junction region between two adjacent **transistor** gate stacks, disposing oxygen and nitrogen in region, and implanting dopant in region.
DC L03 U11
IN IBOK, E
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6153486 A 20001128 (200109)* 6p
ADT US 6153486 A Provisional US 1999-169693P 19991207, US 2000-479504 20000107
PRAI US 1999-169693P 19991207; US 2000-479504 20000107
AB US 6153486 A UPAB: 20010213

NOVELTY - Semiconductor device (2) is fabricated by establishing **transistor** gate stacks (16) on a substrate (14) so that at least one prospective junction region is defined in the substrate between two adjacent stacks; disposing oxygen and then nitrogen in the region to let nitrogen agglomerate at the peak and define a diffusion boundary; and implanting dopant into the region.

DETAILED DESCRIPTION - Fabrication of semiconductor device comprises: establishing plural **transistor** gate stacks on the substrate so that at least one prospective junction region is defined in the substrate between two adjacent stacks; disposing oxygen in the region; disposing the nitrogen into the region so that the nitrogen agglomerates at the peak to define a diffusion boundary; and implanting dopant into the region. The oxygen defines a concentration profile with peak spaced from the substrate surface by a predetermined distance. The nitrogen impedes the dopant from diffusing past the boundary.

USE - The method is used for fabricating semiconductor device for use as **integrated circuits** and as flash memory for hand held computing devices, wireless telephones, and digital cameras.

ADVANTAGE - The method causes speed-limiting junction capacitance. Therefore undesired electrical capacitance from **source** and **drain regions** and junctions is minimized.

DESCRIPTION OF DRAWING(S) - The drawing shows a side view of a portion of the semiconductor device during oxide implantation.

Semiconductor device 12
Substrate 14
Gate stacks 16
Buried oxide layer 18
Dwg.2/4

L68 ANSWER 21 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2000-664163 [64] WPIX

DNN N2000-492134 DNC C2000-201172
TI Metal oxide semiconductor field-effect **transistor** for **microelectronic** technology includes buried contacts on substrate, an oxide layer on the first buried contact, and extended **source/ drain regions**.
DC L03 U11 U12
IN WU, S
PA (TEXI) TEXAS INSTR ACER INC
CYC 1
PI US 6127712 A 20001003 (200064)* 10p
ADT US 6127712 A CIP of US 1998-83610 19980522, US 1999-346041 19990706
PRAI US 1999-346041 19990706; US 1998-83610 19980522
AB US 6127712 A UPAB: 20001209

NOVELTY - A metal oxide semiconductor field-effect **transistor** (MOSFET) includes two buried contacts on a silicon substrate adjacent the sides of a gate dielectric layer; an oxide layer on the first contact; and extended **source/drain regions**. The poly gate and second buried contact form air gaps on two unoccupied gate dielectric layers.

DETAILED DESCRIPTION - A MOSFET with buried contacts and air-gap gate structure comprises a silicon substrate (102) with trench isolation regions (104) to define an active region; a poly gate (180a) formed of a polysilicon layer (180) in a mid portion of a gate dielectric layer so that there are two unoccupied gate dielectric layer at the sides of polysilicon layer; two buried contacts (140a-b) on the substrate adjacent on sides of the gate dielectric layer; an oxide layer (230) on top of the first buried contact, the poly gate and the second buried contact forming air gaps (235a-b) on the unoccupied gate dielectric layers (170a-b); two **source/drain regions** (240a-b) in the active region underneath the two buried contacts; and two extended **source /drain regions** (250a-b) being extended from the **source/drain regions** to **regions** underneath the unoccupied gate dielectric layers.

USE - The MOSFET is used for **microelectronic** technology.

ADVANTAGE - The ultra-short channel MOSFET is achieved in clarity defined by gate hollow. The device speed is improved due to reduced parasitic resistance by the extended source/drain junction and the parasitic gate fringe capacitor and the capacitance between source/drain and gate is lowered by the air-gaps gate structure. The size of the **transistor** is reduced due to forming buried contacts on both the source/**drain** and STI **region**.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the MOSFET structure.

Silicon substrate 102
Trench isolation regions 104
Buried contacts 140a-b
Gate dielectric layers 170a-b
Polysilicon layer 180
Poly gate 180a
Oxide layer 230
Air gaps 235a-b
Source/drain regions 240a-b
Extended **source/drain regions** 250a-b
Dwg.14/14

L68 ANSWER 22 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2000-611326 [58] WPIX
DNN N2000-452738 DNC C2000-182844
TI Ion-sensitive sensor useful in pH sensors comprises an ion-sensitive surface on an oxide-protected backside of field-effective **transistor**.

12/04/2002

DC A25 L03 S03 U12
IN WALKER, H W
PA (WALK-I) WALKER H W; (DYNA-N) DYNAMICS RES CORP
CYC 21
PI WO 2000051180 A1 20000831 (200058)* EN 15p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CA JP
US 2002031854 A1 20020314 (200222)
US 6387724 B1 20020514 (200239)
ADT WO 2000051180 A1 WO 2000-US4532 20000223; US 2002031854 A1 US 1999-258716 19990226; US 6387724 B1 US 1999-258716 19990226
PRAI US 1999-258716 19990226
AB WO 200051180 A UPAB: 20001114

NOVELTY - A silicon-on-insulator (SOI) sensor comprises a silicon oxide sensing surface on an oxide-protected backside of field-effect **transistor** (FET).

DETAILED DESCRIPTION - An ion-sensitive FET sensor (I) comprises (a) an active silicon layer (1) having source and **drain** diffusion **regions** of FET, (b) a patterned layer of silicon oxide (2) on one side of (1), (c) a patterned layer of metal (3) on (2), (d) an insulative support material layer (4) on (3), and (e) a continuous layer of silicon oxide (5) on the other side of (1). (2) has openings over the **source** and diffusion **regions** of (1). (3) includes two metal contacts respectively formed at and respectively contacting the source and **drain** diffusion **regions** of (1). (5) is exposed in the region of FET such that surface charge is formed in the exposed area, when placed in contact with an electrolyte solution.

An INDEPENDENT CLAIM is also included for fabrication of (I) by (i) forming FET on (1) of SOI **wafer**. (1) is separated from a substrate silicon layer by a **buried** silicon **oxide** layer, (ii) then forming (4) over (1), and (iii) finally removing the substrate silicon layer to expose the **buried** silicon **oxide** layer.

USE - In sensing devices such as pH sensors.

ADVANTAGE - The ion-sensitive FET sensors maintains the required sealing of source and drain contacts without requiring encapsulants. Due to its structure the sensor can be easily integrated with other CMOS (Complementary Metal-Oxide Semiconductor) circuitry, which enables the electrical and packaging aspects of a sensor system to be improved.

DESCRIPTION OF DRAWING(S) - The figure is a schematic view of the silicon-on-insulator (SOI) **wafer** and field-effect **transistor** (FET) after the removal of the substrate silicon and bonding of an insulative support material on the top of the **wafer**
.

buried oxide layer 12
patterned silicon oxide layer 16
metal layer 18
polyimide layer 20
Dwg.3/3

L68 ANSWER 23 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2000-601410 [57] WPIX
CR 1999-539758 [45]
DNN N2000-444983 DNC C2000-179892
TI **Transistor** manufacture using substrate having silicon-on-insulator (SOI) structure and including etching and chemical-mechanical polishing techniques.
DC L03 U11 U12
IN WU, S
PA (TEXI) TEXAS INSTR ACER INC
CYC 1

PI US 6117712 A 20000912 (200057)* 10p
ADT US 6117712 A CIP of US 1998-42348 19980313, US 1999-248955 19990212
FDT US 6117712 A CIP of US 5956580
PRAI US 1999-248955 19990212; US 1998-42348 19980313
AB US 6117712 A UPAB: 20001109
NOVELTY - The manufacture includes etching, chemical-mechanical polishing and doping processes.

DETAILED DESCRIPTION - Process comprises forming **buried oxide** and pad oxide layers (8) on substrate (2) to generate silicon layer (6) in between, patterning silicon nitride layer (10) with a 1st opening on pad oxide layer, forming thermal oxide layer (14) to shrink silicon layer, forming spacers (16) on side walls of opening (12), etching thermal oxide layer using spacers as mask to form 2nd opening, forming dielectric layer on silicon nitride layer, forming metal (alloy) layer on dielectric layer in 2nd opening, performing chemical-mechanical polishing to form a gate in 2nd opening, removing silicon nitride layer and spacers adjacent thermal oxide layer, performing 1st ion implantation to form source and drain next to gate, activating dopants in source and drain by thermal annealing, removing pad oxide and thermal oxide layers, performing 2nd ion implantation to form lightly doped **drain** (LDD) **structure** next to **drain** and forming 2nd spacers on gate side walls.

USE - Used to form MOSFETs with ultra-short channels and elevated source and drain on an ultra-thin SOI substrate.

ADVANTAGE - High performance **integrated circuits** can be formed with high package density.

DESCRIPTION OF DRAWING(S) - The drawings show the cross-section of a semiconductor **wafer** during the various stages of manufacture of the **transistor**.

Substrate 2
SOI structure 4
Silicon layer 6
Pad oxide layer 8
Silicon nitride layer 10
Opening 12
Thick field oxide 14
Sidewall spacers 16
4, 13, 15/15

L68 ANSWER 24 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2000-145644 [13] WPIX
DNN N2000-413416
TI Lateral bipolar mode FET for high frequency and high voltage **ICs**, has buried insulation layer, drift **region**, **source region**, **drain region** and gate region.
DC U12
IN KIM, S D
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD; (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 3
PI KR 99006170 A 19990125 (200013)*
JP 2000243756 A 20000908 (200048) 6p
US 6084254 A 20000704 (200052)B 9p
US 6358786 B1 20020319 (200224)
ADT KR 99006170 A KR 1997-30392 19970630; JP 2000243756 A JP 1998-183894 19980630; US 6084254 A US 1998-105397 19980626; US 6358786 B1 Div ex US 1998-105397 19980626, US 2000-591965 20000612
FDT US 6358786 B1 Div ex US 6084254
PRAI KR 1997-30392 19970630
AB US 6084254 A UPAB: 20001018 ABEQ treated as Basic
NOVELTY - A drift region (22) with preset conductivity is formed on a buried insulation layer (21) formed on a substrate. A gate region (24)

with preset conductivity formed in the drift region is separated from the insulation layer at a specific distance. A **source region** contacting the gate region is formed over the insulation layer. The **drain region** located opposite the **source region** is separated from the gate region at a selected distance.

USE - Used to manufacture bipolar mode field effect **transistor** (BMFET) formed on a silicon-on-insulation (SOI) substrate suitable for a **integrated circuit** in high frequency and high voltage applications.

ADVANTAGE - Obtains very few forward voltage drop and high switching compared with conventional metal oxide silicon gate lateral power device. Larger current gain and larger current capability are obtained by gate region.

DESCRIPTION OF DRAWING(S) - The figure shows the perspective view of a lateral silicon on insulator bipolar mode field effect **transistor**.

Buried insulation layer 21
Drift region 22
Gate region 24
Dwg.2/5

AB KR 99006170 A UPAB: 20001023
NOVELTY - A drift region (22) with preset conductivity is formed on a buried insulation layer (21) formed on a substrate. A gate region (24) with preset conductivity formed in the drift region is separated from the insulation layer at a specific distance. A **source region** contacting the gate region is formed over the insulation layer. The **drain region** located opposite the **source region** is separated from the gate region at a selected distance.

USE - Used to manufacture bipolar mode field effect **transistor** (BMFET) formed on a silicon-on-insulation (SOI) substrate suitable for a **integrated circuit** in high frequency and high voltage applications.

ADVANTAGE - Obtains very few forward voltage drop and high switching compared with conventional metal oxide silicon gate lateral power device. Larger current gain and larger current capability are obtained by gate region.

DESCRIPTION OF DRAWING(S) - The figure shows the perspective view of a lateral silicon on insulator bipolar mode field effect **transistor**.

Buried insulation layer 21
Drift region 22
Gate region 24
Dwg.2/5

L68 ANSWER 25 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1999-481466 [41] WPIX
DNN N1999-358617 DNC C1999-141812
TI Electrode temperature control structure in **chip** size package - includes solder bump formed on electrode provided on insulating layer of substrate.
DC A26 A85 L03 U11
IN HIRANO, Y; MAEDA, S; MAEGAWA, S; NISHIMURA, T; TSUTSUMI, K
PA (MITQ) MITSUBISHI DENKI KK; (MITQ) MITSUBISHI ELECTRIC CORP; (HIRA-I) HIRANO Y; (MAED-I) MAEDA S; (MAEG-I) MAEGAWA S; (NISH-I) NISHIMURA T; (TSUT-I) TSUTSUMI K
CYC 6

PI	FR 2775387	A1	19990827	(199941)*	22p
	DE 19842441	A1	19990909	(199943)	
	JP 11243208	A	19990907	(199947)	7p
	KR 99071421	A	19990927	(200048)	
	TW 382817	A	20000221	(200050)	

US 2002003259 A1 20020110 (200208)
KR 2001072669 A 20010731 (200209)
US 2002110954 A1 20020815 (200256)
US 6459125 B2 20021001 (200268)
ADT FR 2775387 A1 FR 1998-11927 19980924; DE 19842441 A1 DE 1998-19842441 19980916; JP 11243208 A JP 1998-45459 19980226; KR 99071421 A KR 1998-44987 19981027; TW 382817 A TW 1998-112003 19980723; US 2002003259 A1 US 1998-122863 19980727; KR 2001072669 A KR 2001-4231 20010130; US 2002110954 A1 Div ex US 1998-122863 19980727, US 2002-122322 20020416; US 6459125 B2 US 1998-122863 19980727
PRAI JP 1998-45459 19980226
AB FR 2775387 A UPAB: 19991122

NOVELTY - A semiconductor device has a semiconductor layer (120) formed within an insulating layer (107, 108) and including a **transistor** of SOI structure.

DETAILED DESCRIPTION - A semiconductor device comprises a semiconductor layer (120) formed in an insulating layer (107, 108) and including a **transistor** of SOI structure, an electrode (103, 105, 106) formed on the insulating layer and a conductive bump (11) formed on the electrode. INDEPENDENT CLAIMS are also included for the following: (i) production of a semiconductor device by successively forming an electrode (103, 105, 106) on a semiconductor substrate (101), a conductive bump (11) on the electrode and an alpha -radiation blocking insulating film on the substrate surface except for the electrode; (ii) a semiconductor device comprising an electrode (103, 105, 106) formed on a semiconductor substrate (101), a conductive bump (11) formed on the electrode, an alpha -radiation blocking film covering the substrate surface except for the electrode, a first element which is located in a substrate zone which extends in line of sight from the bump and which is not masked by the film, and a second element which is located outside the zone and which is less resistant to alpha -radiation than the first element; and (iii) a semiconductor device comprising an electrode (103, 105, 106) formed on a semiconductor substrate (101), a conductive bump (11) formed on the electrode, an alpha -radiation blocking film covering the substrate surface except for the electrode, an insulating oxide film which is located in a substrate zone which extends in line of sight from the bump and which is not masked by the alpha -radiation blocking film, and an element which is located in the substrate outside the zone.

USE - Especially as a **chip** size package (CSP) for mounting on a printed circuit board.

ADVANTAGE - The design ensures that alpha -radiation generates electrons and holes in quantities which do not affect **transistor** functioning and ensures a low probability of crack formation in the semiconductor layer as a result of differential thermal expansion between the circuit board and the CSP.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a semiconductor device structure according to the invention.

Solder bump 11 alpha -radiation 91
Holes 92
Electrons 93
Semiconductor substrate 101
Aluminum pad 103
Silicon nitride film 104
Titanium layer 105
Nickel layer 106
Buried oxide film 107
Interlayer insulation film 108
Gate electrode 110
Semiconductor layer 120
Transistor source/drain regions 120a, b

Dwg.1/14

L68 ANSWER 26 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1997-023501 [03] WPIX
CR 1996-211367 [22]; 1997-366174 [34]
DNN N1997-019498 DNC C1997-007637
TI Formation of raised **source / drain regions** in **integrated circuits** - by applying poly silicon and a planar layer to a gate electrode, etching back revealing field oxide and doping the remaining poly silicon.
DC L03 U11
IN CHAN, T C; SMITH, G C
PA (SGSA) SGS THOMSON MICROELTRN INC; (SGSA) STMICROELECTRONICS INC
CYC 6
PI EP 747941 A2 19961211 (199703)* EN 11p
R: DE FR GB IT
JP 09008303 A 19970110 (199712) 9p
US 5683924 A 19971104 (199750) 10p
US 5955770 A 19990921 (199945)
ADT EP 747941 A2 EP 1996-303952 19960531; JP 09008303 A JP 1996-143078 19960605; US 5683924 A CIP of US 1994-331691 19941031, US 1995-486347 19950607; US 5955770 A CIP of US 1994-331691 19941031, Div ex US 1995-486347 19950607, US 1997-877911 19970618
FDT US 5955770 A Div ex US 5683924
PRAI US 1995-486347 19950607; US 1994-331691 19941031; US 1997-877911 19970618
AB EP 747941 A UPAB: 19991103
A gate electrode is formed over a gate oxide which overlies a substrate, the gate electrode being electrically isolated by many field oxide regions. A capping layer is formed over the gate electrode and LDD regions formed in the adjacent substrate. Sidewall spacers are formed on the gate electrodes and doped polysilicon raised **source / drain regions** are formed over the LDD **regions**. The raised **source / drain regions** are formed by applying additional polysilicon and a planar sacrificial layer and etching them back to reveal the field oxide surface, leaving a portion of polysilicon adjacent to the gate electrodes. The remaining polysilicon is then doped as required.

Also claimed are **integrated circuits** using **transistors encapsulated** in **dielectrics** to replace the gate oxide and gate electrodes.

USE - This invention relates to **integrated circuit** processing, in particular a method of forming planar **transistors**
.

ADVANTAGE - This invention provides a method of forming planar **transistors** while producing raised **source / drain regions** of low resistivity providing reduced junction leakage and preventing shorting.
Dwg.11/11

L68 ANSWER 27 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1997-023500 [03] WPIX
CR 1996-395257 [40]
DNN N1997-019497 DNC C1997-007636
TI Field effect **transistor structure** with isolated **source-drain regions** - using a dielectric layer beneath these regions to isolate them from the body greatly reducing latch up and preventing spiking.
DC L03 U11 U12 U13
IN BLANCHARD, R A
PA (SGSA) SGS THOMSON MICROELTRN INC; (SGSA) STMICROELECTRONICS INC

12/04/2002

CYC 6
PI EP 747940 A2 19961211 (199703)* EN 12p
R: DE FR GB IT
JP 09022950 A 19970121 (199713) 13p
US 5773328 A 19980630 (199833)
US 5981318 A 19991109 (199954)
US 6291845 B1 20010918 (200157)
ADT EP 747940 A2 EP 1996-303349 19960513; JP 09022950 A JP 1996-133424 19960528; US 5773328 A CIP of US 1995-397654 19950228, US 1995-474710 19950607; US 5981318 A CIP of US 1995-397654 19950228, Div ex US 1995-474710 19950607, US 1997-993679 19971218; US 6291845 B1 CIP of US 1995-397654 19950228, Div ex US 1995-474710 19950607, Div ex US 1997-993679 19971218, US 1999-382403 19990824
FDT US 5773328 A CIP of US 5668025; US 5981318 A CIP of US 5668025, Div ex US 5773328; US 6291845 B1 CIP of US 5668025, Div ex US 5773328, Div ex US 5981318
PRAI US 1995-474710 19950607; US 1995-397654 19950228; US 1997-993679 19971218; US 1999-382403 19990824
AB EP 747940 A UPAB: 20011005

IC devices formed by:

(i) covering part of the surface of a monolithic semiconductor by a dielectric layer leaving material exposed in **transistor** channel locations;

(ii) additional semiconductor material is then formed, monocrystalline in the channels and polycrystalline elsewhere, the layer thickness being greater than the dielectric layer;

(iii) an oxidising species is implanted in the channel regions forming a **buried dielectric** layer while the additional material is patterned to form a patterned thin film layer, on which a gate dielectric is formed;

(iv) a patterned conductive layer is formed on the gate dielectric and dopants are implanted in the additional material not masked by the conductive layer.

Where the monocrystalline regions of additional material beneath the conductive layer provide adjacent **source** and **drain regions**.

Also claimed is a CMOS device where the substrate has at least one region of each conductivity type.

USE - This invention relates to **IC**, particularly latch up resistant CMOS devices.

ADVANTAGE - The advantages of this device are;

(i) reduced capacitance between the **source** and **drain regions**;

(ii) reduced **source** / **drain region** spacings;

(iii) spiking through **source** / **drain regions** is prevented by a dielectric layer beneath them;

(iv) latch up is reduced as the **source** / **drain regions** do not contact the body;

(v) the design can be incorporated in complex process sequences such as BiCMOS technology or used in technologies including NMOS, PMOS, CMOS, DMOS or JFET.

Dwg.7/8

L68 ANSWER 28 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1996-301795 [31] WPIX
DNN N1996-253960
TI Semiconductor device with thin film silicon on insulator MOSFET - has impurity layer with high concn. in semiconductor substrate formed below buried insulation layer with MOSFET channel and **source-drain regions** formed above buried insulation layer.

DC U11 U12 U13 U14 U21
IN EIMORI, T; MATSUFUSA, J; NISHIMURA, T; OASHI, T
PA (MITQ) MITSUBISHI DENKI KK; (MITQ) MITSUBISHI ELECTRIC CORP
CYC 5
PI DE 19548076 A1 19960627 (199631)* 35p
JP 08181316 A 19960712 (199638) 21p
TW 297941 A 19970211 (199721)
CN 1130808 A 19960911 (199801)
US 5721444 A 19980224 (199815) 34p
ADT DE 19548076 A1 DE 1995-19548076 19951221; JP 08181316 A JP 1994-319684 19941222; TW 297941 A TW 1995-102322 19950311; CN 1130808 A CN 1995-119435 19951221; US 5721444 A Cont of US 1995-576352 19951221, US 1997-824550 19970325
PRAI JP 1994-319684 19941222
AB DE 19548076 A UPAB: 19960808
The semiconductor device includes a substrate (1b) with a main surface in which is formed a buried insulation layer (2) in a position separate from the main surface. Also provided is a LOCOS insulating film (3b), a thin film **transistor**, and an impurity layer (15). The LOCOS film is provided in the main surface of the semiconductor substrate to insulate one active region from another active region.

The thin-layer **transistor** is formed in the active region and it has a gate electrode (8) on one active region with an intermediate gate insulating layer (7). Also provided is a pair of source/drain layers (5) in the substrate main surface on both sides of the gate electrode, and a channel region (4). The impurity layer is formed in the substrate with a high concentration impurity and it is directly under the buried layer. Pref. the thin-layer **transistor** is of planar or mesa type.

USE/ADVANTAGE - For DRAM with large capacity, e.g. 256 M, or **logic circuit**. Thin-film SOI-MOSFET prevents generation of ''buckel'' current, or current in OFF state due to weaker inversion region being provided by work function between impurity layer and MOSFET channel region.
Dwg.6/50

L68 ANSWER 29 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1994-146678 [18] WPIX
DNN N1994-115592
TI Insulated gate bipolar **transistor** - has insulated gate extend in buried from source surface through base, and has emitter terminal connected to base contact which overlaps source.
DC U12
IN SUMIDA, H
PA (FJIE) FUJI ELECTRIC CO LTD
CYC 3
PI GB 2272572 A 19940518 (199418)* 47p
JP 06151838 A 19940531 (199426) 7p
JP 07094724 A 19950407 (199523) 7p
GB 2272572 B 19960710 (199631) 1p
US 5572055 A 19961105 (199650) 15p
US 5624855 A 19970429 (199723) 15p
JP 3206149 B2 20010904 (200152) 7p
JP 3206289 B2 20010910 (200155) 7p
ADT GB 2272572 A GB 1993-22665 19931103; JP 06151838 A JP 1992-297500 19921109; JP 07094724 A JP 1994-75217 19940414; GB 2272572 B GB 1993-22665 19931103; US 5572055 A Cont of US 1993-145848 19931105, US 1995-491517 19950619; US 5624855 A Div ex US 1993-145848 19931105, Cont of US 1994-238694 19940505, US 1995-491686 19950619; JP 3206149 B2 JP 1992-297500 19921109; JP 3206289 B2 JP 1994-75217 19940414
FDT JP 3206149 B2 Previous Publ. JP 06151838; JP 3206289 B2 Previous Publ. JP 07094724

PRAI JP 1992-297500 19921109; JP 1993-142413 19930615
AB GB 2272572 A UPAB: 19940622
The **transistor** includes a base layer (22) of opposite conductivity diffused from a surface of a semiconductor region (12), with a source layer (23) diffused in a surface area of the base layer and into the semiconductor region. There is a collector layer (26), of the same conductivity as the base layer, diffused from a surface of the semiconductor region on the opposite side of an insulated gate (25) w.r.t. the source layer.

The insulated gate is buried in a surface recess (24) which extends from the source layer surface through the base layer into the semiconductor region. There is an emitter terminal E connected to the base layer and the source layer, a collector terminal C connected to the collector layer, and a gate terminal G connected to the insulated gate. Pref. there is a base contact layer diffused on the base layer surface, so that it overlaps an edge of the base layer and contacts the source layer, with the emitter terminal drawn from the base layer through the base contact.

USE/ADVANTAGE - Horizontal IGBT for **integrated circuit**. Prevents latch-up; reduced turn-off time.
Dwg.3a/10

L68 ANSWER 30 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1993-207189 [26] WPIX
CR 1992-260872 [32]; 1994-357466 [44]
DNN N1993-159365 DNC C1993-091766
TI High voltage, thin film **transistor** - has drift region shielded from external electric fields and contg. linear doping profile and field plate.
DC L03 U11 U12
IN MERCHANT, S; MERCHANT, S L
PA (PHIG) PHILIPS GLOEILAMPENFAB NV; (PHIG) PHILIPS ELECTRONICS NV; (PHIG) NORTH AMERICAN PHILIPS CORP; (PHIG) PHILIPS ELECTRONICS NORTH AMERICA CORP
CYC 7
PI EP 549042 A2 19930630 (199326)* EN 4p
R: DE FR GB IT NL
US 5246870 A 19930921 (199339) 5p
JP 05259456 A 19931008 (199345) 4p
EP 549042 A3 19931006 (199510)
US 5412241 A 19950502 (199523) 5p
EP 549042 B1 19970312 (199715) EN 6p
R: DE FR GB IT NL
DE 69218155 E 19970417 (199721)
ADT EP 549042 A2 EP 1992-203924 19921215; US 5246870 A CIP of US 1991-650391 19910201, US 1991-811554 19911220; JP 05259456 A JP 1992-337036 19921217; EP 549042 A3 EP 1992-203924 19921215; US 5412241 A CIP of US 1991-650391 19910201, Cont of US 1991-811554 19911220, US 1993-101164 19930803; EP 549042 B1 EP 1992-203924 19921215; DE 69218155 E DE 1992-618155 19921215, EP 1992-203924 19921215
FDT US 5412241 A Cont of US 5246870; DE 69218155 E Based on EP 549042
PRAI US 1991-811554 19911220; US 1991-650391 19910201; US 1993-101164 19930803
AB EP 549042 A UPAB: 19950102
Thin film SOI device comprises: a **buried oxide** layer (2); a thin Si layer (1) having a lateral linear doping region (4) on the oxide layer (2); top oxide layer (6) on the Si layer (1); gate region (7) at one thin layer (1) end; **drain region** (10) at the other thin layer (1) end; and a **source region** (10) laterally sepd. from the gate region (7). The gate region includes a gate electrode (7) and field plate (7) extending from the electrode over the doping region (4).

USE/ADVANTAGE - The gate electrode, overlying the drift region protects it from external fields caused by moisture or charged contaminents on the **wafer** surface, which are terminated on the field plate. The drift region may be depleted from the top and bottom, so twice the conducting charge may be placed on the drift region, lowering the on-resistance.
Dwg.1/2
Dwg.1/2
Dwg.1/2

L68 ANSWER 31 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1992-260872 [32] WPIX
CR 1993-207189 [26]; 1994-357466 [44]
DNN N1992-199476 DNC C1992-116497
TI Mfr. of **integrated circuit** devices by semiconductor-on-insulator technology - for high voltage application improving voltage breakdown.
DC L03 U11 U12
IN ARNOLD, E; MERCHANT, S; MERCHANT, S L
PA (PHIG) PHILIPS ELECTRONICS NV; (PHIG) PHILIPS GLOEILAMPENFAB NV; (PHIG) NORTH AMERICAN PHILIPS CORP; (PHIG) US PHILIPS CORP
CYC 7
PI EP 497427 A2 19920805 (199232)* EN 11p
R: DE FR GB IT NL
JP 04309234 A 19921030 (199250) 8p
EP 497427 A3 19930310 (199349)
US 5300448 A 19940405 (199413) 11p
EP 497427 B1 19960410 (199619) EN 13p
R: DE FR GB IT NL
DE 69209678 E 19960515 (199625)
US 5767547 A 19980616 (199831)
ADT EP 497427 A2 EP 1992-200252 19920129; JP 04309234 A JP 1992-15324 19920130; EP 497427 A3 EP 1992-200252 19920129; US 5300448 A Cont of US 1991-650391 19910201, US 1993-15061 19930208; EP 497427 B1 EP 1992-200252 19920129; DE 69209678 E DE 1992-609678 19920129, EP 1992-200252 19920129; US 5767547 A Cont of US 1991-650391 19910201, Div ex US 1993-15061 19930208, Cont of US 1993-165602 19931209, US 1995-448268 19950523
FDT DE 69209678 E Based on EP 497427; US 5767547 A Div ex US 5300448
PRAI US 1991-650391 19910201; US 1993-15061 19930208; US 1993-165602 19931209; US 1995-448268 19950523
AB EP 497427 A UPAB: 19971006
A method of mfg. a high voltage thin film **transistor** in a thin layer of monocrystalline silicon provided over an oxide layer on silicon substrate, comprises: forming a mask with numerous openings of progressively increasing dimensions over the thin layer of silicon and introducing impurities into the silicon through the openings forming numerous doped regions of different width. The mask is then removed and the layer is annealed to form a nearly linear doping profile over the silicon. A **transistor** structure is formed with the silicon layer having a linear doping profile.

A high voltage thin film silicon-on-insulator **transistor** is claimed comprising: a thin layer of monocrystalline silicon of first conductivity having a linear doping profile from one side to the other, and the thin layer on a **buried oxide** layer on a silicon substrate, an oxide layer over the thin layer, a polysilicon gate region in contact with the second conductivity portion, a **source region** adjacent to gate **region**, a **drain region** in contact with first conductivity type, and electrodes disposed through oxide layer contacting the source, gate and **drain regions**.

USE/ADVANTAGE - **Integrated circuit** devices

manufactured by semiconductor-on-insulator technology exhibiting improved voltage breakdown, esp. for very thin (less than 1 micron) films.
Dwg.11/16

L68 ANSWER 32 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1991-101663 [14] WPIX
DNN N1991-078583 DNC C1991-043585
TI Radiation-hardened CMOS on SOI or SOS devices - has end plugs preventing parasitic **transistor** effects being induced by gamma radiation.
DC L03 U11 U13
IN BAHRAMAN, A
PA (USAF) US SEC OF AIR FORCE
CYC 1
PI US 5001528 A 19910319 (199114)*
ADT US 5001528 A US 1989-304759 19890131
PRAI US 1989-304759 19890131
AB US 5001528 A UPAB: 19930928
A radiation hardened MOS SOI or SOS **transistor** with end plugs comprises an SOI or SOS **wafer** on which are similarly doped source (2a) and **drain** (2b) **regions** with an oppositely doped channel (3) contiguous to and between them. End plugs (6) connect to the channel and extend along opposite ends of the source, and have the same dopant type as the channel but at higher concn. and the electrical connections are established to drain, channel, source and each of the end plugs.

Pref. a silica region (7) isolates the **transistor**, which is pref. NMOS or PMOS. Pref. there is a layer of **buried oxide** (4) between the **wafer** (6) and **source** and channel **regions**. pref. the end plugs are of Si.

USE/ADVANTAGE - A radiation-hardened MOS SOI or SOS **transistor** (claimed) is provided. The body is electrically tied to the source, thus preventing a bipolar **transistor** operation being turned on by gamma rays. Also end plugs separate the MOS sidewalls from an isolation oxide, thus preventing a radiation turn-on of the sidewall **transistor**. Radiation hardness can be coupled with high device density and the end plugs add little to **chip** area in e.g. random logic LSI/VLSI devices. @(5pp Dwg.No.1/4)@

L68 ANSWER 33 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1989-093405 [12] WPIX
DNN N1989-071096
TI J-MOS **transistor** utilising poly silicon sinks - includes poly silicon layer having portions serving as gate for depleting channel and collector for minority carriers.
DC U12
IN JAIN, K C; MACIVER, B A; VALERI, S J
PA (GENK) GENERAL MOTORS CORP
CYC 1
PI US 4811063 A 19890307 (198912)* 10p
ADT US 4811063 A US 1987-110453 19871020
PRAI US 1987-110453 19871020
AB US 4811063 A UPAB: 19930923
The **transistor** includes a monocrystalline silicon **chip** within which are formed **source** and **drain** **regions** of one conductivity type spaced apart along a channel of the same conductivity type. A polysilicon layer includes a portion positioned along the channel and insulated for serving as the gate for depleting the channel.

A second portion includes device for collecting minority carriers from the channel when the first portion is at a gate potential for depleting the channel. The devices for collecting the minority carriers

are back-to-back P-N junctions in the second portion of the polysilicon layer.
ADVANTAGE - More efficiency. Elimination of need for **buried oxide** layer.
2A/6

L68 ANSWER 34 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1988-051054 [08] WPIX
DNN N1988-038775
TI Forming buried insulating layers in semiconductor substrate - in which selected sections are preset and insulating layer forming substance is implanted.
DC U11
IN COLINGE, J P; KAMINS, T I; MARCOUX, P J; MOLL, J L; ROYLANCE, L M
PA (HEWP) HEWLETT-PACKARD CO; (YOKH) YOKOGAWA HEWLETT PACKARD LTD
CYC 3
PI DE 3726842 A 19880218 (198808)* 12p
JP 63072164 A 19880401 (198819)
US 4810664 A 19890307 (198912) 11p
ADT DE 3726842 A DE 1987-3726842 19870812; JP 63072164 A JP 1987-200766 19870811; US 4810664 A US 1986-896560 19860814
PRAI US 1986-896560 19860814
AB DE 3726842 A UPAB: 19930923
The buried insulating layers are formed in selected sections for a semiconductor substrate (10). At the preset positions, oxygen is implanted forming the insulating layers (28,30). A mask (24) blocks the implantation of the oxygen with the exception of in the required areas.
The mask may contain tungsten or a nitride. The process is used for the mfr. of a MOS **transistor** with a source and a **drain zone** formed in the semiconductor substrate, while between them is formed a gate structure on the substrate. The buried insulating layers are located under the **source** and **drain zones**.
ADVANTAGE - Reduced capacitance between **integrated circuit** and substrate, and reduced leakage currents. Reduced cost and mfg. time.
3/8

L68 ANSWER 35 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1987-067154 [10] WPIX
DNN N1987-050924 DNC C1987-027896
TI Forming buried interconnect esp. in silicon-on-insulator structure - by forming substrate doped region before depositing device semiconductor layer.
DC L03 U11
IN TZENG, J C
PA (ITLC) INTEL CORP
CYC 5
PI GB 2179787 A 19870311 (198710)*
FR 2586509 A 19870227 (198714)
JP 62047151 A 19870228 (198714)
CN 86102300 A 19870225 (198820)
US 4778775 A 19881018 (198844) 7p
GB 2179787 B 19890920 (198938)
ADT GB 2179787 A GB 1986-5289 19860304; FR 2586509 A FR 1986-4377 19860326; JP 62047151 A JP 1986-166858 19860717; US 4778775 A US 1987-54806 19870527
PRAI US 1985-769019 19850826; US 1987-54806 19870527
AB GB 2179787 A UPAB: 19930922
An interconnect is formed in a substrate for devices fabricated in a semiconductor layer formed over an insulating layer over the substrate by: forming a doped region in the substrate before forming the semiconductor layer over the insulating layer; forming an opening through the insulating

layer over the doped region; and depositing a semiconductor layer over the opening so that the doped region forms an interconnect.
USE/ADVANTAGE - Esp. in mfr. of MOS devices, esp. those using Si on insulators. Interconnect is formed within the substrate itself for use with devices in the overlying semiconductor layer.
6/8

L68 ANSWER 36 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 2002-033490 JAPIO
TI MANUFACTURING METHOD FOR SOI-MOS FIELD-EFFECT **TRANSISTOR**
IN GO TEIKI
PA HYNIX SEMICONDUCTOR INC
PI JP 2002033490 A 20020131 Heisei
AI JP 2001-170062 (JP2001170062 Heisei) 20010605
PRAI KR 2000-200037414 20000630
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To improve a change effect in a threshold voltage(Vt) generated in the formation of a semiconductor **integrated circuit** and to improve a parasitic bipolar effect.
SOLUTION: A **buried oxide** film 11 and an active silicon film 12 are formed sequentially on an SOI substrate 10. A first photoresist film 13 is formed. A recess channel region 14 is formed by an ion implantation process. The recess channel region is etched, and a dummy spacer 15 is formed on its sidewall. A gate 16 is formed on the recess channel region. A second photoresist film 17 is formed in the upper part of the active silicon film and the gate. Ions are implanted. An LDD region 14a is formed. Low-concentration impurity ions are implanted, and a low-concentration ion region 18 is formed. A spacer 19 is formed on the sidewall of the recess channel region. High-concentration impurity ions are implanted into the active silicon film. A **source region** 20 and a **drain region** 21 are formed. A source/drain electrode and a gate electrode are formed.
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L68 ANSWER 37 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 2000-243756 JAPIO
TI HORIZONTAL BIPOLAR FIELD EFFECT **TRANSISTOR** AND MANUFACTURE THEREOF
IN KIM SEONG-DONG
PA HYUNDAI ELECTRONICS IND CO LTD
PI JP 2000243756 A 20000908 Heisei
AI JP 1998-183894 (JP10183894 Heisei) 19980630
PRAI KR 1997-30392 19970630
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To obtain a horizontal SOIBMFET which is suitable for an **IC** by a method, wherein a drift region is formed on the top surface of an buried insulating film, a gate region is arranged apart from the drift **region**, and a **drain region** is formed confronting a **source region** separate from the gate region.
SOLUTION: A lightly-doped N--type drift region 52 is epitaxially grown on the top surface of a **buried oxide** film 51 on a semiconductor substrate 50, and then an oxide film 53 is formed thereon, and a trench T is cut in the drift region 52. A heavily-doped P+-type gate region 54 is formed separate from the trench T by a prescribed space. The gate region 54 is formed above the top surface of the **buried oxide** film 51 by a distance d corresponding to a channel depth. Then, an N-type **source region** 55 is formed between the trench T and the gate region 54. An N+-**drain region** 56 is formed counterposing the **source region** 55 separated

from the gate region 54 by a prescribed distance, at the same time as when the **source region** 55 is formed.
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L68 ANSWER 38 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1999-289052 JAPIO
TI BURIAL TYPE THERMAL CONDUCTOR FOR SEMICONDUCTOR **CHIP**
IN RAJEEV BASANT JOSHI; WILLIAM ROBERT LEO
PA INTERNATL BUSINESS MACH CORP <IBM>
PI JP 11289052 A 19991019 Heisei
AI JP 1999-5031 (JP11005031 Heisei) 19990112
PRAI US 1998-6575 19980113
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To reduce the operating temperature of each element by burying a thermal conductor into a semiconductor **chip** structure, forming a plurality of elements in the structure adjacent to the thermal conductor, and transferring heat that is generated in the elements through the thermal conductor.
SOLUTION: With a semiconductor **chip** structure 200, oxygen is implanted deeply into a substrate 210, a **buried oxide** layer 212 is formed, reactive ion etching is made to the lower portion, an opening for a shallow trench is formed, and a diamond thermal conductor 202 that is grown in contact with the substrate 210 in the shallow trench is glued to a recessed **region** near a **source** 230 and a drain 232. Then, a plurality of elements such as a **transistor**, a resistor are formed adjacent to the diamond thermal conductor 202, and heat that is generated in the elements is transferred through the diamond thermal conductor 202, thus reducing the operating temperature of each element.
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L68 ANSWER 39 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1988-072164 JAPIO
TI MANUFACTURE OF IMPROVED TYPE **INTEGRATED CIRCUIT**
IN SEODOORU AI KAMINZU; JIEN PIERU KORINJI; PAURU JIEE MARUKOUKUSU; RIN EMU ROIRANSU; JIYON ERU MORU
PA YOKOGAWA HEWLETT PACKARD LTD
PI JP 63072164 A 19880401 Showa
AI JP 1987-200766 (JP62200766 Showa) 19870811
PRAI US 1986-896560 19860814
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1988
AB PURPOSE: To realize the implantation of a patterned oxide layer into a semiconductor device and to improve the resisting characteristics regarding a source and drain capacity, a high-speed operation and a floating parent body by a method wherein, after a prescribed pattern mask has been attached to a substrate, an oxide-forming substance is irradiated onto the surface where the mask is attached so that a **buried oxide** layer can be formed at a prescribed position within the substrate.
CONSTITUTION: By attaching a patterned mask composed of a high-density material to the surface of a device, the implantation of oxygen is blocked selectively. For this purpose, a tungsten layer 24 is attached to a polysilicon gate 20 and a polysilicon connection path 22 by means of a chemical vapor deposition method at 300°C. Then, a substrate 10 is irradiated with oxygen ions or oxygen molecules so that a **buried oxide** layer 28 and a **buried** drain **oxide** layer 30 can be formed. This MOS **transistor** contains a **source region** 32 and a **drain region** 34 electrically insulated respectively from the oxide layers 28, 30, via the substrate 10, as well as a parent body region under a channel region 36 which is electrically connected to the substrate 10 via an opening 38 located

between the edges of the source oxide layer 28 and the drain oxide layer 30. Through this constitution, an **integrated circuit** of high performance can be obtained.
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L68 ANSWER 40 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1984-130457 JAPIO
TI COMPLEMENTARY TYPE FIELD EFFECT SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN ANADA IKUO; SATO YOICHI; ONO KAZUMASA; MUKAI HISAKAZU
PA OKI ELECTRIC IND CO LTD
NIPPON TELEGR & TELEPH CORP <NTT>
PI JP 59130457 A 19840727 Showa
AI JP 1984-2 (JP59000002 Showa) 19840104
PRAI JP 1984-2 19840104
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1984
AB PURPOSE: To contrive to increase the density and increase VTH while preventing the cut of a wiring caused by the stepwise difference of an oxide film by a method wherein a thick Si **oxide** layer is **buried** deeply into a substrate between MOS **transistors**.
CONSTITUTION: A P type substrate 11 becomes the substrate of the channel type **transistor**, and an N type **source** and **drain region** 12a and 12b are formed therein. On the other hand, as the substrate of the P-channel type MOS **transistor**, an N-well 13 built in the P type substrate 11 is used, and the **source** and **drain regions** 14a and 14b of the P type MOS **transistor** are formed therein. An oxidized porous part 15 is formed by heat treatment in a high temperature oxygen atmosphere containing steam. A C-MOS **integrated circuit** of such a structure can be largely reduced in shape by the presence of the layer 15 produced by oxidizing porous Si. Since the layer 15 has a structure of burial under the surface of the substrate, the surface is flattened, and the trouble due to the cut of an Al film, etc. is eliminated, further the integration density increases.
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L68 ANSWER 41 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1982-188845 JAPIO
TI MASTER SLICED SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN MATSUKUMA MOICHI
PA NEC CORP
PI JP 57188845 A 19821119 Showa
AI JP 1981-74402 (JP56074402 Showa) 19810518
PRAI JP 1981-74402 19810518
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1982
AB PURPOSE: To decrease load capacitance, to improve the characteristics of the device and to ameliorate the degree of integration by directly connecting each wiring layer to the source, **drain** and gate **regions** of an MOS type **transistor**.
CONSTITUTION: A field oxide film 12 is formed onto a semiconductor substrate 11, and the MOS type **transistor** consisting of the source and the drain 20, a gate oxide film and a polysilicon gate is shaped onto an element forming region. Polysilicon having high impurity concentration is formed to the extracting sections of the source and the drain 20 in the same manner as the gate section, and platinum silicide layers 22 are shaped to the surfaces. Sections among these layers are **buried** by **oxide** films 21, and flattened. The first layer metallic film 23 is molded, an insulating film 24 is grown, a desired contact hole 25 is formed, and the second layer metallic film 26 is directly connected to the silicide layer 22 without through the first layer metallic film. Accordingly, the metallic films of each layer

mutually become independent, and can be contacted from the same surface.
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